

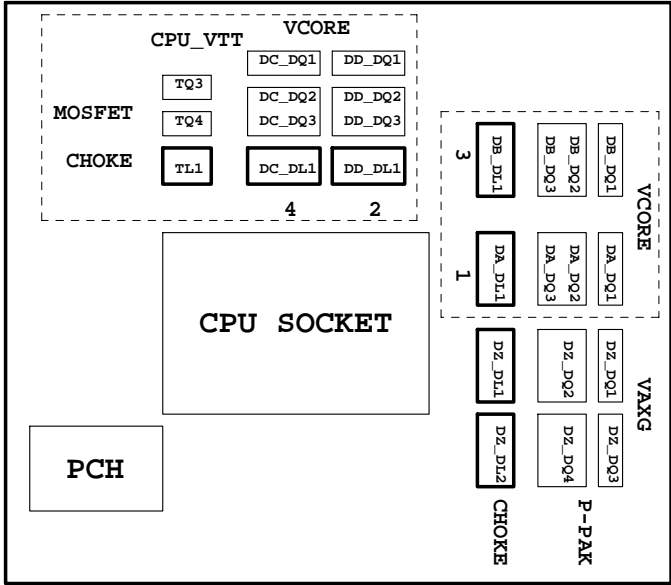
# Model Name: GA-Z77-D3H

SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1155-A
05	CPU_LGA1155-B
06	CPU_LGA1155-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE,NVRAM
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCIEX1*3 , PCIEX4 SLOT
16	ITE8892 PCI BRIDGE
17	PCI SLOT 1&2
18	I/O ITE8728
19	COM, -PROHOT, R_USB
20	Dual BIOS , TPM SLB9635TT
21	VT2021 CODEC
22	REAR AUDIO JACK
23	VCORE PWM_IR3564
24	VCORE PWM DRIVER IR3598
25	NCP3933 OVER VOLTAGE
26	DISCRETE POWER
27	DDR_15V & CPU_VTT PWM IR3570

SHEET TITLE

28	DDR_15V & CPU_VTT PWM DRIVER CHL8550
29	VCCSA POWER
30	F_PANEL , F_USB2.0/3.0
31	ATX POWER, CLOCK GEN
32	HWM , KB/MS , FAN CTRL
33	LAN ATHEROS AR8151
34	N/A
35	M-SATA
36	DVI
37	HDMI , R_USB30
38	TABLE LIST
39	
40	



Gigabyte Technology

Cover Sheet			
Title	GA-Z77-D3H		
Size	Document Number	Rev	1.02
Custom			
Date:	Wednesday, June 06, 2012	Sheet	1 of 38

GA-Z77-D3H

Component value change history

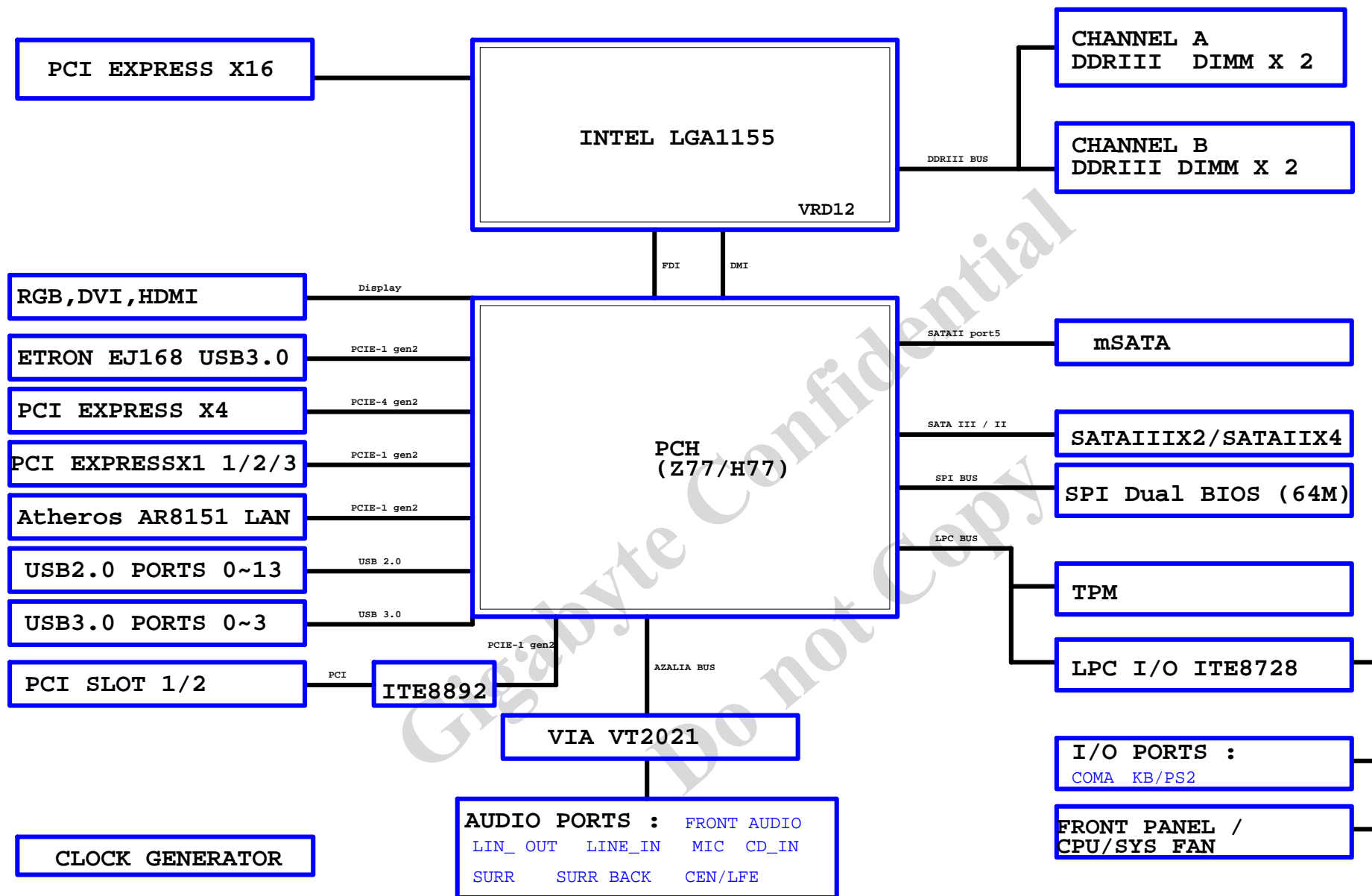
Data	Change Item	Reason
0.1-1124	E-BOM	
02-1216	1. ADD PCH_HS & MOS_HS料號	
	2. PCIE gen2 switch PI3PCIE2415ZHE --> ASM1440	
	3. load-line DAR5=12K , DAR40=1.78K	
10A-0105	1. Z77料號更新	
	2. PWM Driver power vcc or +12v?	
	3. DART2 --> 47K/1/4/S , DAR44 --> 0 ohm	
10B-0113	1. Vcore & VAXG VSEN modify , DAR1,DAR51=100/4/1,DAR2,DAR54=0/4,DAC1,DAC24=3.3nF	
	2. 1.54K加替料:10RC4-001541-22R TA-I	
	1. Remove IR PWM 1X3 pin	
10C-0117	1. DA_DR11,DC_DR11,DZ_DR18 1ohm --> 0ohm	
10D-0119	1. Prochot R65 : 1.65K/4/1 --> 2.74K/4/1	
10E-EVT-0201	1. Modify choke=0.36uH , DRIVER=5V	
10F	1. IR3564要改用新料號03R	
	2. poochot change 100K	
10T	1. 0 OHM Short-pad	
	2. DDR3 FOR OC 2400MHz UP	
10G-1.01	0. PCB Rev1.01 --> ReV1.01 (DDR3 OC 2400MHz+)	
	1. RS_PWM相關線路移除 (若有上prochot pull up改100 ohm)	
	2. Add M/B ID for DDR3 OC	
	3. 固態電容區分100uF/6.3V & 100uF/16V	
10H-1.02	1. PCB Rev1.01 --> ReV1.02 (DDR3 OC 2800MHz+)	
	2. Add M/B ID for DDR3 OC	
	3. ADD DC79 FOR A_CPUPWROK	
	4. 100u 16V-->6.3V	
10I-0430	1. PWM IR3564 --> IR3564A	
	2. Remove DAESD1	
	3. RJK0393DPA 10IF9-040393-01R --> 10IF9-040393-11R	

Circuit or PCB layout change

DATE	Change Item	Reason
P67X-UD3-B3		
2011/02/18-0.1	1. 移除LAR11 ,LAR14 , NR28 ,新增NTP11	
2011/02/18-1.0	2. 新增DR388,DR389,DR391 ; Remove DQ49,DR347,DR371 3. CR44改成R0603-RH 4. R1,LAR3,RBR20,LABC25 -->R0402-2-SHORT 5. RAQ1 --> Q_TO223-MASK 6. RARN1 --> R8P4R-0402-SHORT 7. CESD1-5 --> SSOP5 8. RAQ2,RAEC1一起往下移40mil 9. CESD2文字面要標pin1	
2011/03/8-1.01	1. Add "Dolby" logo	
2011/03/8-1.02	1. UAFB1,UAFB2,UBF1,UBF2 Footprint update 1206-->1812 2. Add "AD1" FOR 5VSB	
Z68XP-D3		
1.0	1. update MINI_PCIE footprint 2. 文字面 : SLOT部分全對齊	
Z77-D3H-0.1	EVT	
0.2-1216	1. Remove SE9172 , Add VCC3 內層(注意其他內層power,跨切割) 2. SPDIF AGND --> GND 3. PCI SLOT & PCIEX1/X4 CAP COST DOWN 4. 0 ohm --> SHORT PAD 5. REMOVE SMBUS FROM COMP TO SOLDER SIDE IN DR POWER 6. SATA3 connect Change to 90 degree (記得SATA3訊號部分要做挖空) 7. Add "108dB"文字面 8. Remove VCC1_05_PCH & VCC1_8_PCH gate net 9. Add EJ168 R_USB30_1 & F_USB3 10. UAE1/UAE2 NET SWAP 11. 內層+12V要打VIA在COMA處 12. SPDIFO_HDMI走12mil	
1.0	1. SATA2-SATA3文字面要隱藏 2. DART2 移至 DC_DQ1左上方 3. Q7 & DAR31 NET Change	
1.01	1. 0 OHM SHORT PAD (LAN & AUDIO) 2. DDR3 2400MHz OC modify	

# BLOCK DIAGRAM

www.xinxunwei.com 400-800-9990

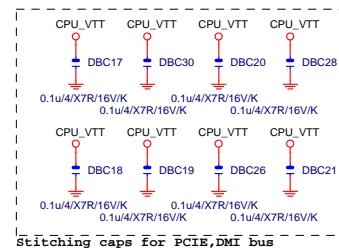
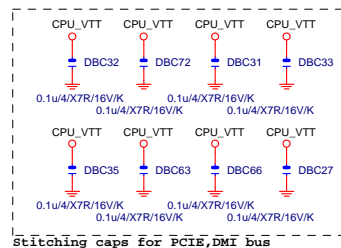
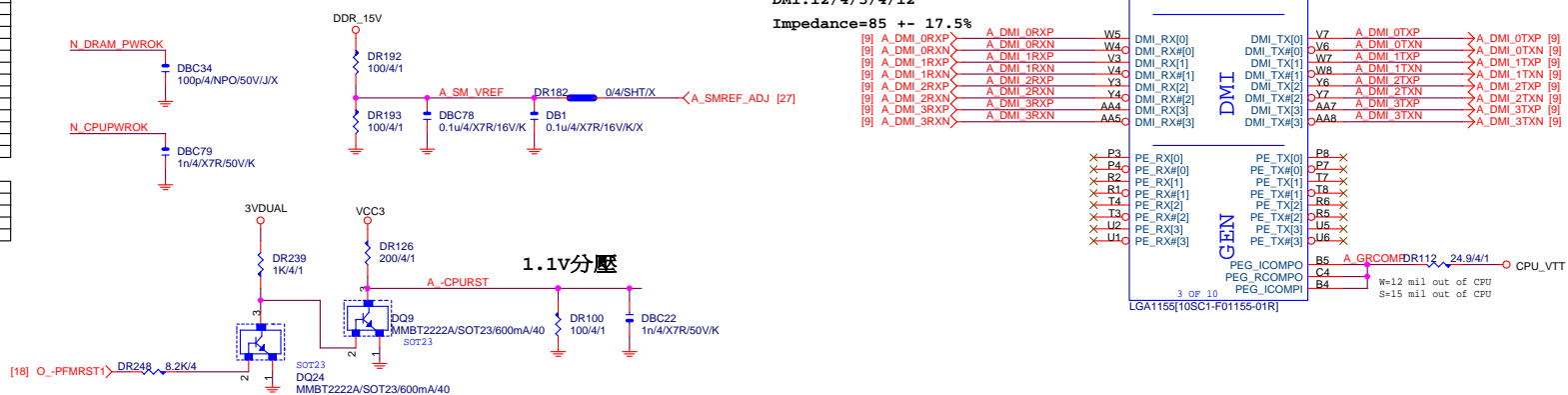




CFG	H	L	NOTE
0	RSVD	RSVD	RSVD
1	RSVD	RSVD	RSVD
2	NOOP	Reverse	LANE REVERSAL[0], x16
3	RSVD	RSVD	RSVD
4	RSVD	RSVD	RSVD
7	RSVD	RSVD	RSVD
8	RSVD	RSVD	RSVD
9	RSVD	RSVD	RSVD
10	RSVD	RSVD	RSVD
11	RSVD	RSVD	RSVD
12	RSVD	RSVD	RSVD
13	RSVD	RSVD	RSVD
14	RSVD	RSVD	RSVD
15	RSVD	RSVD	RSVD
16	RSVD	RSVD	RSVD
17	RSVD	RSVD	RSVD

CFG6	CFG5	PCIe CONFIG
1	1	1x16 , Default
1	0	2X8
0	1	RSVD
0	0	X8,X4,X4

CFG 0-17 all internal PULL-UP



<b>Gigabyte Technology</b>			
Title			
<b>CPU LGA1155-A</b>			
Size	Document Number	<b>GA-Z77-D3H</b>	Rev 1.02
Custom			
Date:	Wednesday, June 06, 2012	Sheet 4 of 38	

## LGA1155A

M_AAA0	AV27	SA_MA[0]	SA_DQ[0]	AK3	M_DQSA0
M_AAA1	AY24	SA_MA[1]	SA_DQ[1]	AK2	M_DQSA0
M_AAA2	AW24	SA_MA[2]			
M_AAA3	AW23	SA_MA[3]			
M_AAA4	AV23	SA_MA[4]	SA_DQ[0]	AJ3	M_DA0
M_AAA5	AT24	SA_MA[5]	SA_DQ[1]	AJ4	M_DA1
M_AAA6	AT23	SA_MA[6]	SA_DQ[2]	AL3	M_DA2
M_AAA7	AU22	SA_MA[7]	SA_DQ[3]	AL4	M_DA3
M_AAA8	AV22	SA_MA[8]	AJ2	M_DA4	
M_AAA9	AT22	SA_MA[9]	AJ1	M_DA5	
M_AAA10	AV28	SA_MA[10]	AL2	M_DA6	
M_AAA11	AU21	SA_MA[11]	AL1	M_DA7	
M_AAA12	AT21				
M_AAA13	AW32	SA_MA[12]	SA_DQ[11]	AP3	M_DQSA1
M_AAA14	AU20	SA_MA[13]	SA_DQ[11]	AP2	M_DQSA1
M_AAA15	AT20	SA_MA[14]			
		SA_MA[15]			

[7] M_SWEA	M_SWEA	AW29	SA_WE#		
[7] M_SCASA	M_SCASA	AV30	SA_DQ[8]	AN1	M_DA8
[7] M_SRASA	M_SRASA	AU28	SA_DQ[9]	AN4	M_DA9
			SA_DQ[10]	AR3	M_DA10
			SA_DQ[11]	AR4	M_DA12
[7] M_SBA0	M_SBA0	AY29	SA_DQ[12]	AN2	M_DA13
[7] M_SBA1	M_SBA1	AW28	SA_DQ[13]	AN3	M_DA13
[7] M_SBA2	M_SBA2	AV20	SA_DQ[14]	AR2	M_DA14
			SA_DQ[15]	AR1	M_DA15

[7] M-CSA0	M-CSA0	AU29	SA_CS#0		
[7] M-CSA1	M-CSA1	AV32	SA_CS#1		
[7] M-CSA2	M-CSA2	AW30	SA_CS#2		
[7] M-CSA3	M-CSA3	AU33	SA_CS#3		

[7] M_CKEA0	M_CKEA0	AV19	SA_CKE[0]		
[7] M_CKEA1	M_CKEA1	AT19	SA_CKE[1]		
[7] M_CKEA2	M_CKEA2	AU18	SA_CKE[2]		
[7] M_CKEA3	M_CKEA3	AV18	SA_CKE[3]		

M_ODT_A0	AV31	SA_ODT[0]			
M_ODT_A1	AU32	SA_ODT[1]			
M_ODT_A2	AU30	SA_ODT[2]			
M_ODT_A3	AW33	SA_ODT[3]			

[7] M_DCLKA0	M_DCLKA0	AY25	SA_CK[0]		
[7] M_DCLKA0	M_DCLKA0	AW25	SA_CK#0		
[7] M_DCLKA1	M_DCLKA1	AU24	SA_CK[1]		
[7] M_DCLKA1	M_DCLKA1	AU25	SA_CK#1		
[7] M_DCLKA2	M_DCLKA2	AW27	SA_CK[2]		
[7] M_DCLKA2	M_DCLKA2	AY27	SA_CK#2		
[7] M_DCLKA3	M_DCLKA3	AW26	SA_CK[3]		
[7] M_DCLKA3	M_DCLKA3	AW26	SA_CK#3		

[7,8] M_DDR3_RST	M_DR1	0.1u4/X7R/16V/K/X	SM_DRAMRST#		

AV13	SA_DQS[8]				
AV12	SA_DQS[8]				
AU12	SA_ECC_CB[0]				
AU14	SA_ECC_CB[1]				
AU13	SA_ECC_CB[2]				
AY13	SA_ECC_CB[3]				
AU11	SA_ECC_CB[4]				
AY12	SA_ECC_CB[5]				
AW12	SA_ECC_CB[7]				

## DDR\_0

1 OF 10

LGA1155[10SC1-F01155-01R]

## LGA1155B

M_AAB0	AK24	SB_MA[0]	SB_DQ[0]	AH7	M_DQSB0
M_AAB1	AM20	SB_MA[1]	SB_DQ[0]	AH6	M_DQSB0
M_AAB2	AM19	SB_MA[2]			
M_AAB3	AK18	SB_MA[3]			
M_AAB4	AP19	SB_MA[4]	SB_DQ[0]	AG7	M_DB0
M_AAB5	AP18	SB_MA[5]	SB_DQ[1]	AG8	M_DB1
M_AAB6	AM18	SB_MA[6]	SB_DQ[2]	AJ9	M_DB2
M_AAB7	AL18	SB_MA[7]	SB_DQ[3]	AJ8	M_DB3
M_AAB8	AY17	SB_MA[8]	SB_DQ[4]	AG5	M_DB5
M_AAB9	AN18	SB_MA[9]	SB_DQ[5]	AG6	M_DB6
M_AAB10	AN13	SB_MA[10]	SB_DQ[6]	AJ6	M_DB6
M_AAB11	AU17	SB_MA[11]	SB_DQ[7]	AJ7	M_DB7
M_AAB12	AT18	SB_MA[12]			
M_AAB13	AR26	SB_MA[13]	SB_DQ[11]	AM8	M_DQSB1
M_AAB14	AY16	SB_MA[14]	SB_DQ[11]	AL8	M_DQSB1
M_AAB15	AV16	SB_MA[15]			

[8] M_SWEB	M_SWEB	AR25	SB_WE#		
[8] M_SCASB	M_SCASB	AK25	SB_DQ[8]	AM7	M_DB8
[8] M_SRASB	M_SRASB	AP24	SB_DQ[9]	AM10	M_DB10
			SB_DQ[10]	AL10	M_DB11
			SB_DQ[11]	AL6	M_DB12
			SB_DQ[12]	AL9	M_DB13
			SB_DQ[13]	AM9	M_DB15
			SB_DQ[14]		
			SB_DQ[15]		

[8] M_SBA0	M_SBA0	AP23	SB_BS[0]		
[8] M_SBA1	M_SBA1	AM2	SB_BS[1]		
[8] M_SBA2	M_SBA2	AW17	SB_BS[2]		

[8] M-CSB0	M-CSB0	AN25	SB_CS#0		
[8] M-CSB1	M-CSB1	AN26	SB_CS#1		
[8] M-CSB2	M-CSB2	AL25	SB_CS#2		
[8] M-CSB3	M-CSB3	AT26	SB_CS#3		

[8] M_CKEB0	M_CKEB0	AU18	SB_CKE[0]		
[8] M_CKEB1	M_CKEB1	AY15	SB_CKE[1]		
[8] M_CKEB2	M_CKEB2	AW15	SB_CKE[2]		
[8] M_CKEB3	M_CKEB3	AV15	SB_CKE[3]		

M_ODT_B0	AL26	SB_ODT[0]			
M_ODT_B1	AP26	SB_ODT[1]			
M_ODT_B2	AM26	SB_ODT[2]			
M_ODT_B3	AK26	SB_ODT[3]			

[8] M_DCLKB0	M_DCLKB0	AL21	SB_CK[0]		
[8] M_DCLKB0	M_DCLKB0	AL22	SB_CK#0		
[8] M_DCLKB1	M_DCLKB1	AL20	SB_CK[1]		
[8] M_DCLKB1	M_DCLKB1	AK20	SB_CK#1		
[8] M_DCLKB2	M_DCLKB2	AL23	SB_CK[2]		
[8] M_DCLKB2	M_DCLKB2	AM22	SB_CK#2		
[8] M_DCLKB3	M_DCLKB3	AP21	SB_CK[3]		
[8] M_DCLKB3	M_DCLKB3	AN21	SB_CK#3		

[8] M_VREF_DQB	M_VREF_DQB	AH1	FC_AH1		
[7] M_VREF_DOA	M_VREF_DOA	AH4	FC_AH4		

AN16	SB_DQS[8]				
AN15	SB_DQS[8]				
AL16	SB_ECC_CB[0]				
AM16	SB_ECC_CB[1]				
AP16	SB_ECC_CB[2]				
AR16	SB_ECC_CB[3]				
AL15	SB_ECC_CB[4]				
AM15	SB_ECC_CB[5]				
AP15	SB_ECC_CB[6]				
AR15	SB_ECC_CB[7]				

SB_DQS[5]	SB_DQS[5]				
SB_DQS[6]	SB_DQS[6]				

AP32	M_DB40				
AP21	M_DB41				
AP35	M_DB42				
AP34	M_DB43				
AR32	M_DB44				
AR31	M_DB45				
AR35	M_DB46				
AR34	M_DB47				

AL33	M_DQSB6				
AM33	M_DQSB6				

SB_DQ[48]	AM32	M_DB48			
SB_DQ[49]	AM31	M_DB49			
SB_DQ[50]	AL35	M_DB50			
SB_DQ[51]	AL32	M_DB51			
SB_DQ[52]	AM34	M_DB52			
SB_DQ[53]	AL31	M_DB53			
SB_DQ[54]	AM35	M_DB54			
SB_DQ[55]	AL34	M_DB55			

AG35	M_DQSB7				
AG34	M_DQSB7				

SB_DQ[56]	AH35	M_DB56			
SB_DQ[57]	AH34	M_DB57			
SB_DQ[58]	AE34	M_DB58			
SB_DQ[59]	AE35	M_DB59			
SB_DQ[60]	AJ35	M_DB60			
SB_DQ[61]	AJ34	M_DB61			
SB_DQ[62]	AE33	M_DB62			
SB_DQ[63]	AE33	M_DB63			

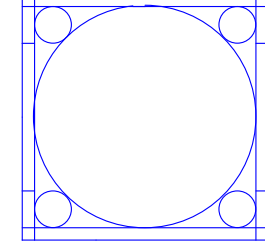
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2 OF 10

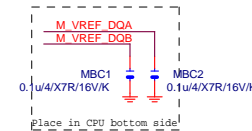
LGA1155[10SC1-F01155-01R]

## LGA1155

ILM BP/1156/CSP

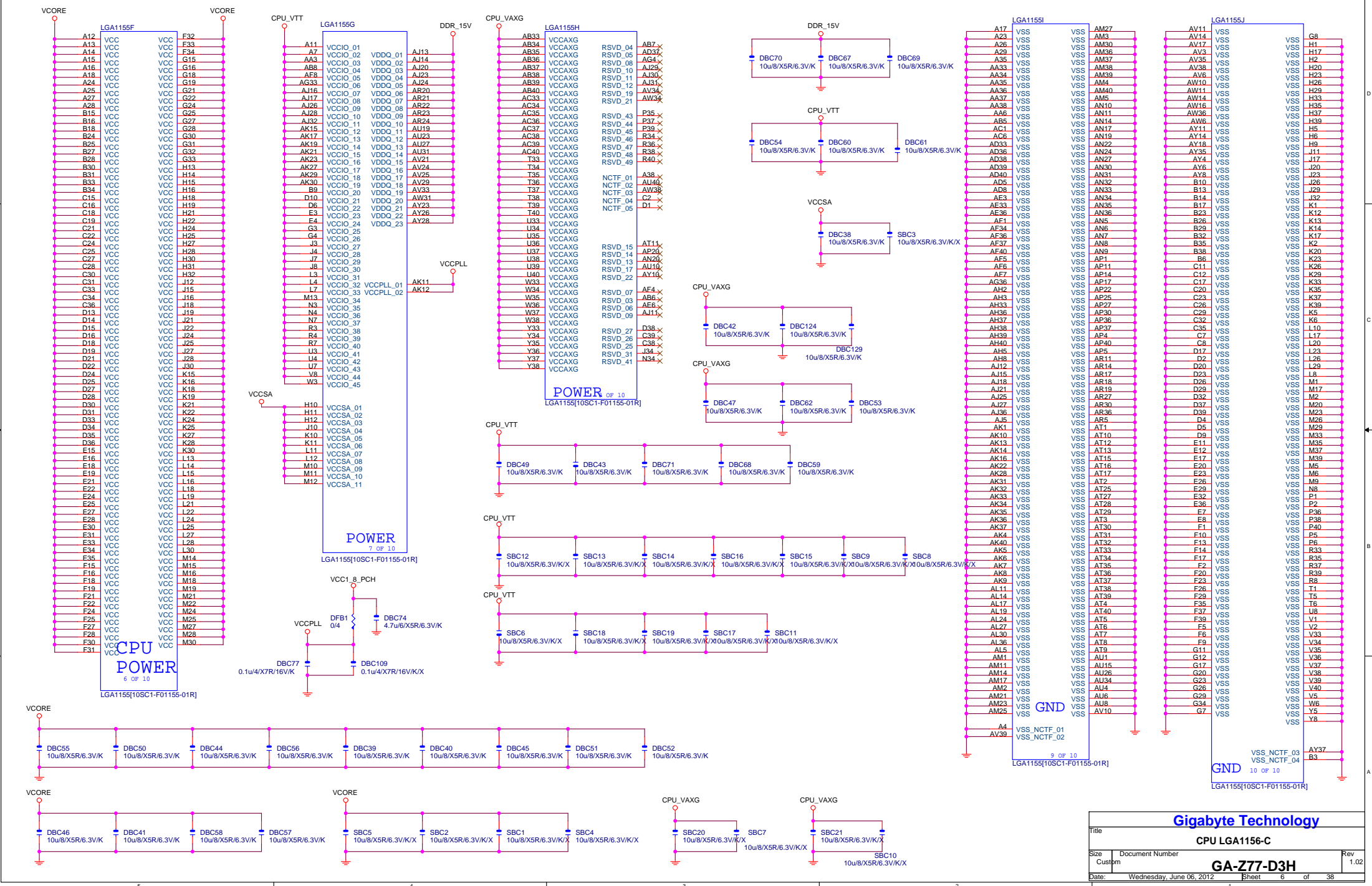


Need check the new CPU ME

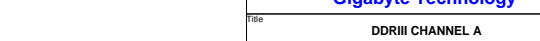


## Gigabyte Technology

Title			CPU LGA1156-B		
Size			Document Number		
Custom			GA-Z77-D3H		
Date:			Wednesday, June 06, 2012		
Sheet			5 of 38		
Rev			1.02		

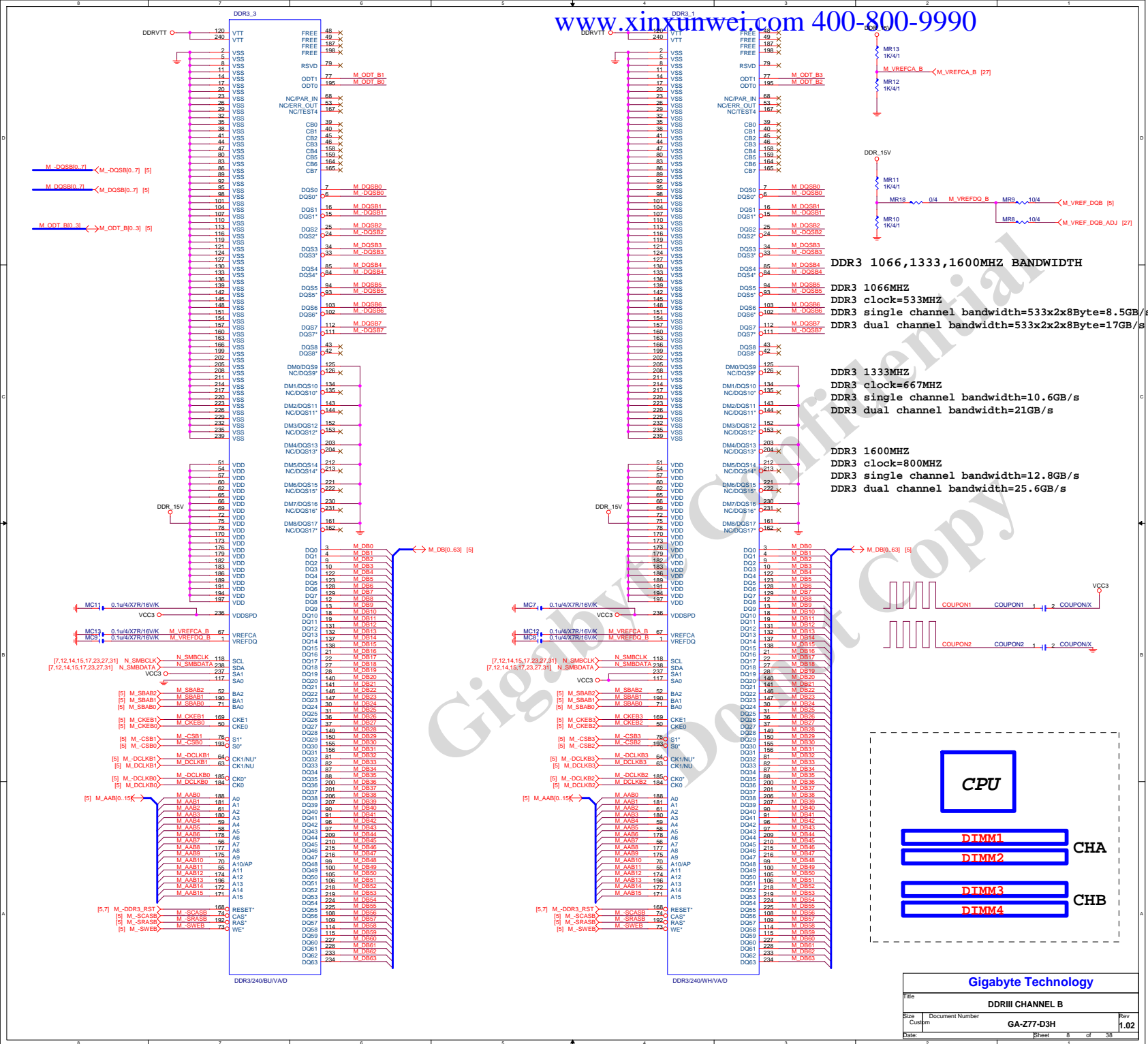






### DDR15V Decouple

### DDRVTT Decouple





USB3.1 30/5/7/5/20 (breakout min 8/4/4/4/8) ; ONLY 3 VIAS  
 Impedance=85 +- 17.5%  
 Back Panel < 10000 MILS  
 Front Panel < 6000 MILS

USB2.0 : 12/4.5/7.5/4.5/12 (breakout min 8/4/4/4/8)  
 Impedance=90 +- 17.5%

PCHB

PCHG

FDILINK

FDI\_RXN0  
 FDI\_RXP0  
 FDI\_RXN1  
 FDI\_RXP1  
 FDI\_RXN2  
 FDI\_RXP2  
 FDI\_RXN3  
 FDI\_RXP3  
 FDI\_RXN4  
 FDI\_RXP4  
 FDI\_RXN5  
 FDI\_RXP5  
 FDI\_RXN6  
 FDI\_RXP6  
 FDI\_RXN7  
 FDI\_RXP7

FDI\_TXN0  
 FDI\_TXP0  
 FDI\_TXN1  
 FDI\_TXP1  
 FDI\_TXN2  
 FDI\_TXP2  
 FDI\_TXN3  
 FDI\_TXP3  
 FDI\_TXN4  
 FDI\_TXP4  
 FDI\_TXN5  
 FDI\_TXP5  
 FDI\_TXN6  
 FDI\_TXP6  
 FDI\_TXN7  
 FDI\_TXP7

FDI:12/4/5/4/12

Impedance=85 +- 17.5%

FDI\_TXP0\_7I >>> FDI\_TXP0[0..7] [4]  
 FDI\_TXN0\_7I >>> FDI\_TXN0[0..7] [4]

PCHE

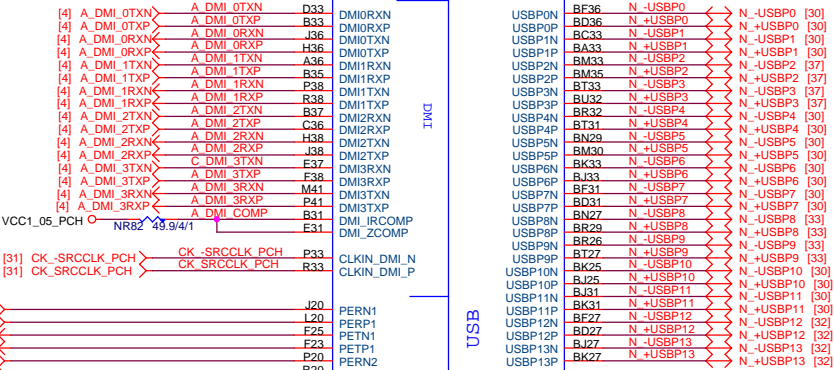
RESERVED\_29  
 DF\_VTS  
 RESERVED\_6  
 RESERVED\_4  
 RESERVED\_3  
 RESERVED\_2  
 RESERVED\_1  
 RESERVED\_22  
 RESERVED\_21  
 RESERVED\_14  
 RESERVED\_13  
 RESERVED\_12  
 RESERVED\_11  
 RESERVED\_10  
 RESERVED\_9  
 RESERVED\_8  
 RESERVED\_7  
 RESERVED\_20  
 RESERVED\_19  
 RESERVED\_18  
 RESERVED\_17  
 RESERVED\_16  
 RESERVED\_15  
 RESERVED\_28  
 RESERVED\_27  
 RESERVED\_26  
 RESERVED\_25  
 RESERVED\_24  
 RESERVED\_23  
 RESERVED\_5  
 K50  
 K49  
 AB46  
 G56  
 Y44  
 L53  
 R50 N NV RCOMP NR155 33/4

BD82Z77/S

OC0#	USB0,1
OC1#	USB2,3
OC2#	USB4,5
OC3#	USB6,7
OC4#	USB8,9
OC5#	USB10,11
OC6#	USB12,13
OC7#	Not Use

Mount for integrated clock Generation Mode

CK\_DOTCLK NR84 8.2K/4  
 CK\_DOTCLK NR88 8.2K/4  
 R102 short to GND in non graphic SKU



USB

PCI-E

2 OF 11

放靠近 Device &amp; PCI-E Slot

PCIEX1:16/5/5/5/16 (breakout min 8/4/4/4/8)

Impedance=80 +- 17.5%

VCC3  
 NBC51  
 1u/4/X5R/6.3V/K

N-USBOC\_F  
 NBC45  
 0.1u/4/X7R/16V/K

N-USBOC\_R  
 NBC46  
 0.1u/4/X7R/16V/K

3VDUAL  
 NR98  
 8.2K/4

N\_GPIO14

PCH\_HS

1X

VCC1\_8\_PCH

NR118 2.2K/4/1

NR117 4.7K/4 N NV CLE

A\_H\_SNB [4]

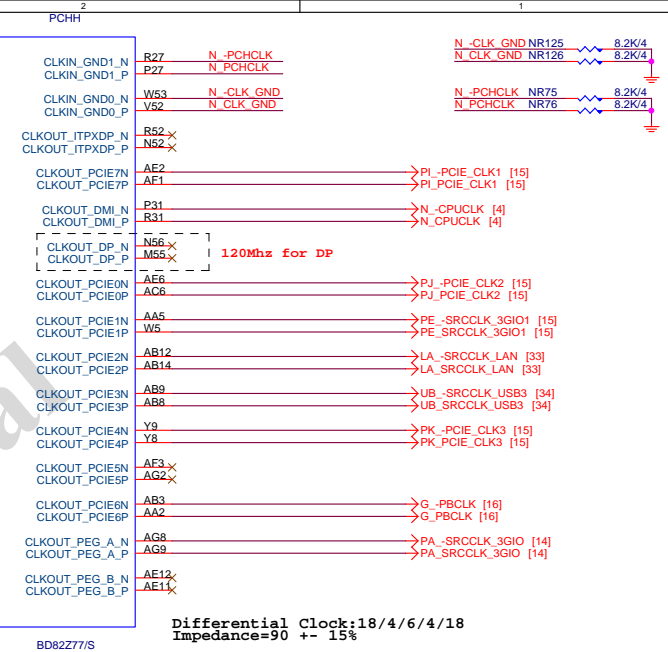
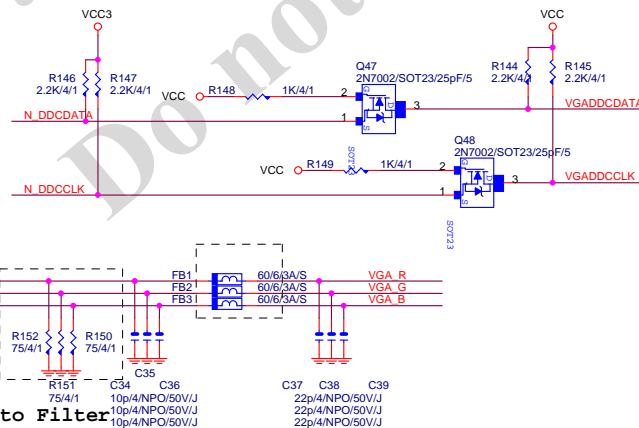
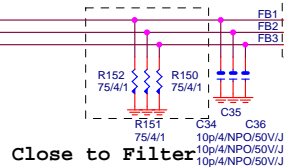
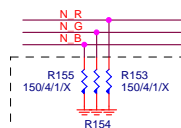
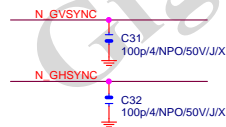
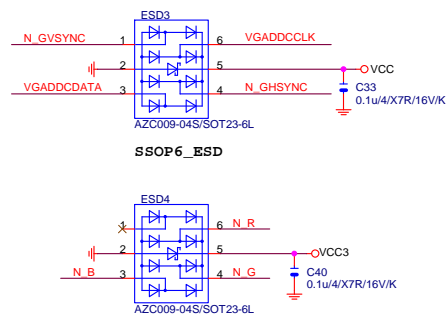
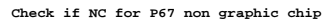
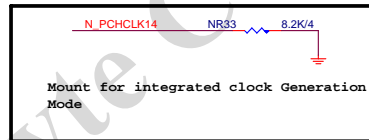
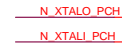
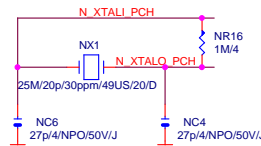
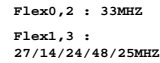
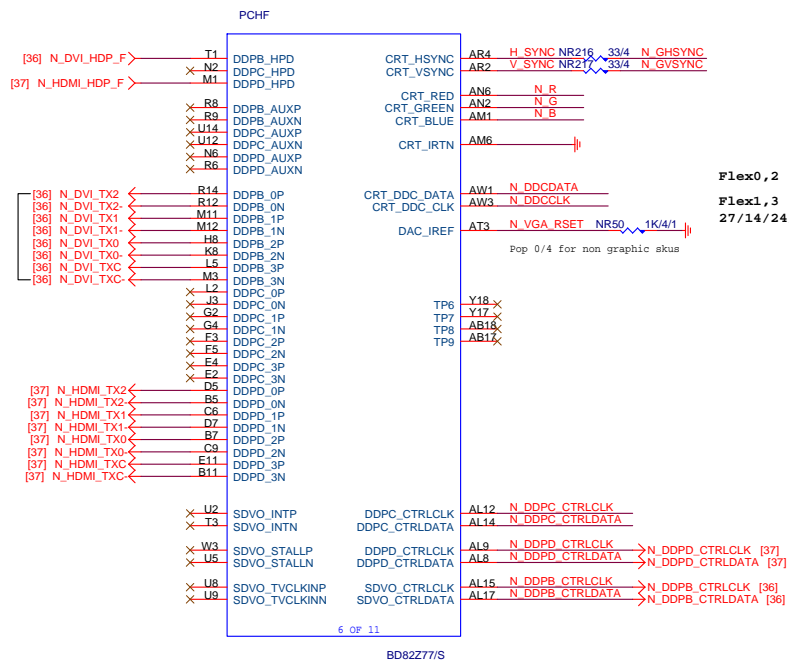
DMI / FDI termination voltage

NBC57 0.1u/4/X7R/16V/K

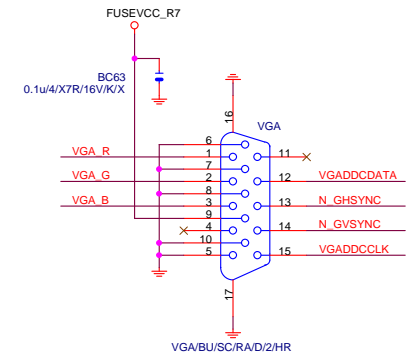
NPCH\_HS[12SP2-S05511-01R\_12SP2-S05511-02R\_12SP2-S05511-03R]

Gigabyte Technology

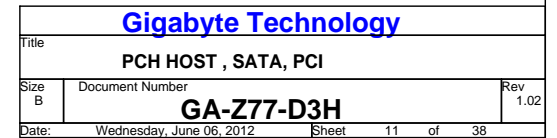
Title		
PCH FDI,DMI,USB,PCI-E		
Size	Document Number	Rev
Custom	GA-Z77-D3H	1.02
Date:	Wednesday, June 06, 2012	Sheet 9 of 38

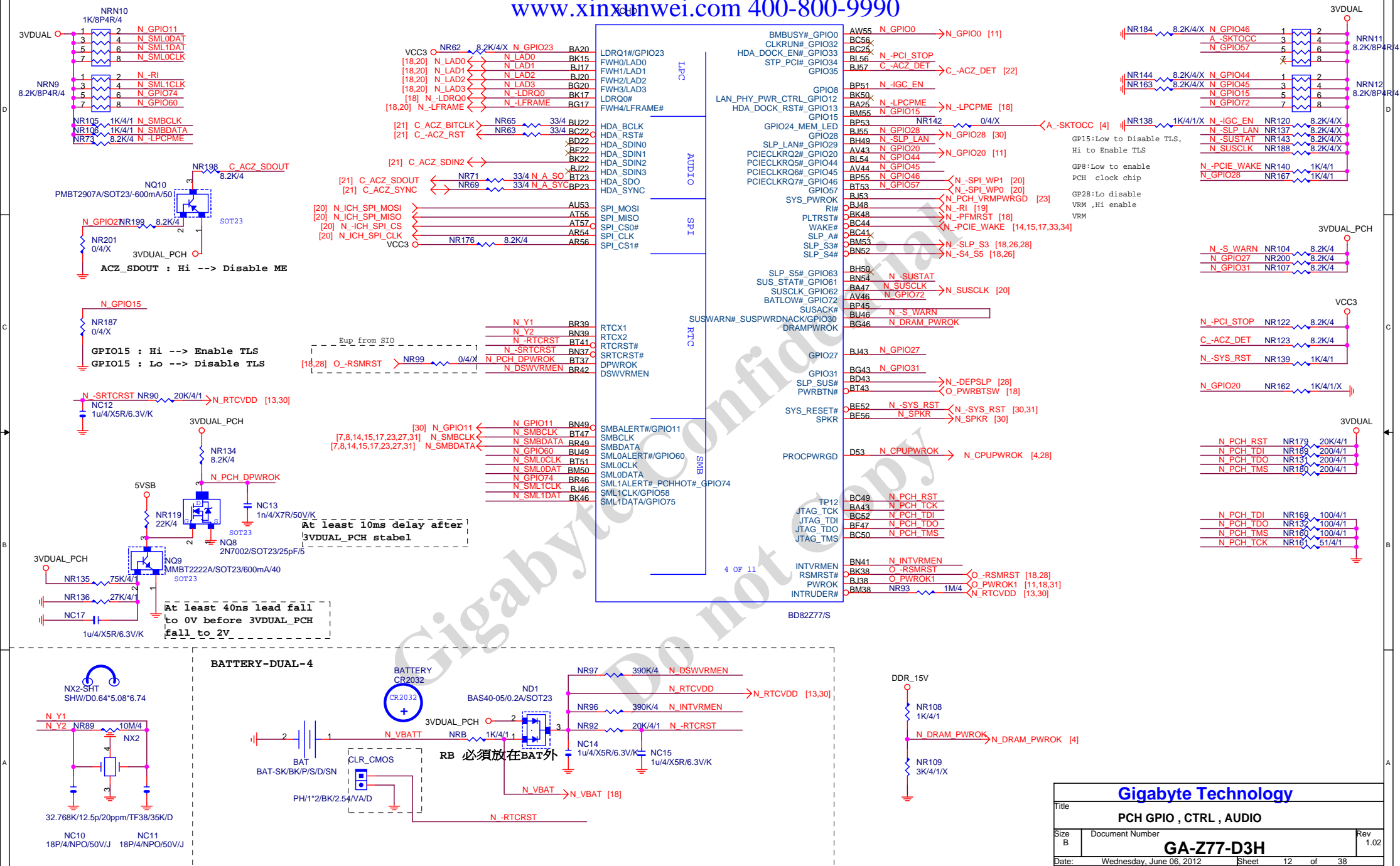


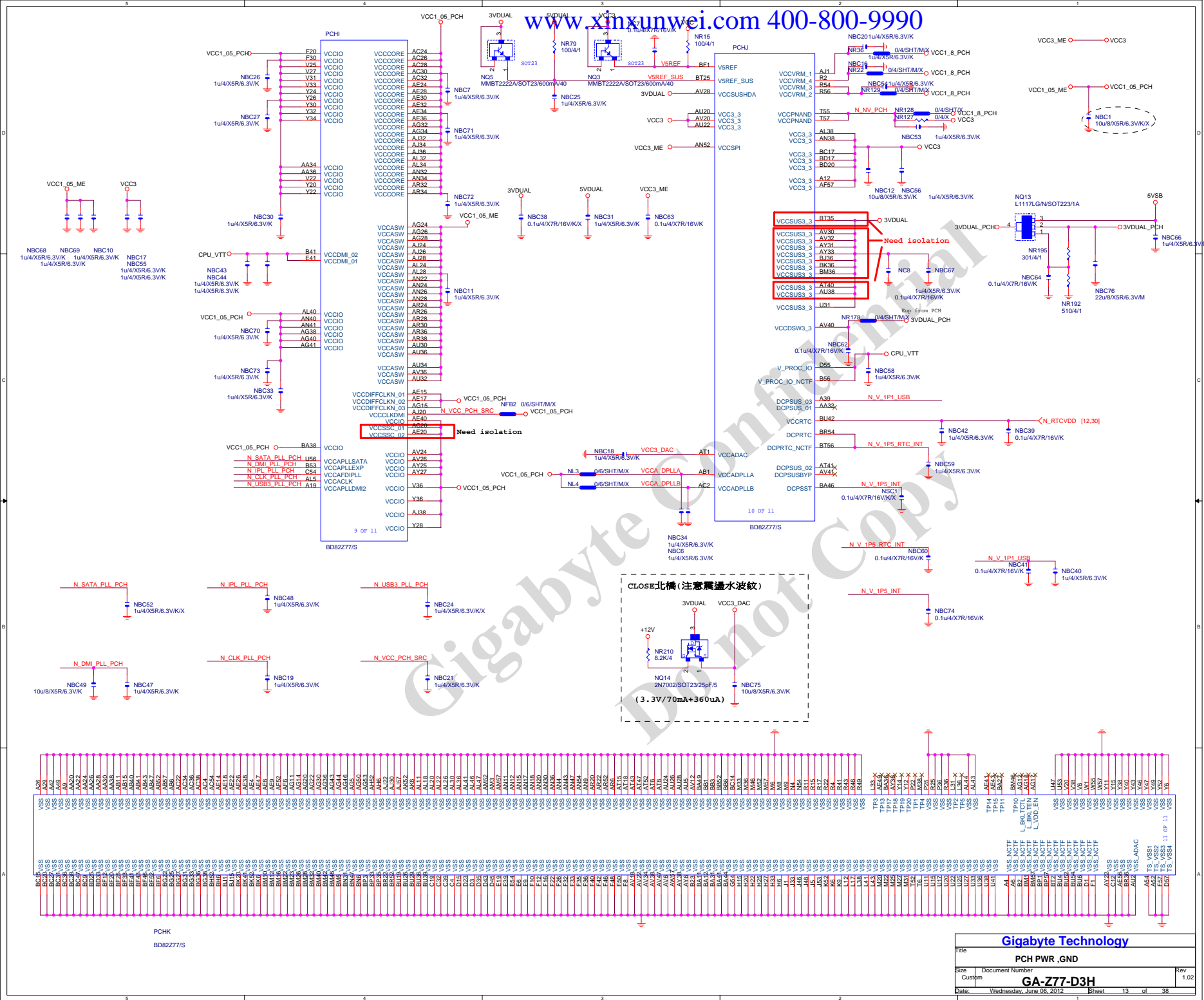
Differential Clock:18/4/6/4/18  
Impedance=90 +- 15%



NR64 8.2K/4/X N\_GPIO17  
NR173 8.2K/4/X N\_GPIO19





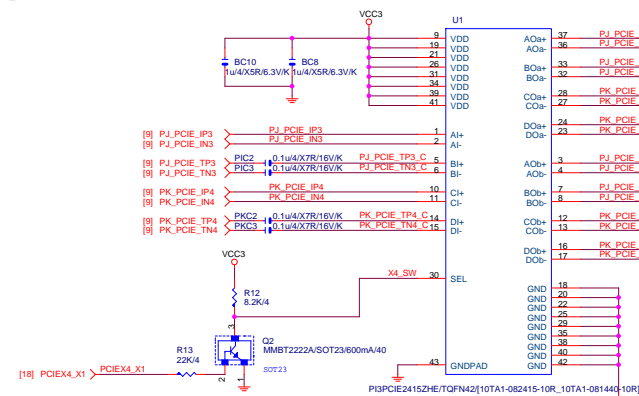
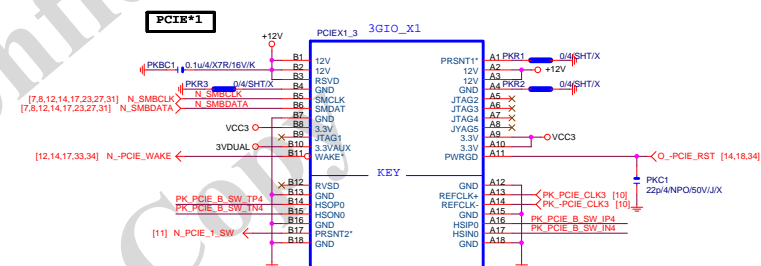
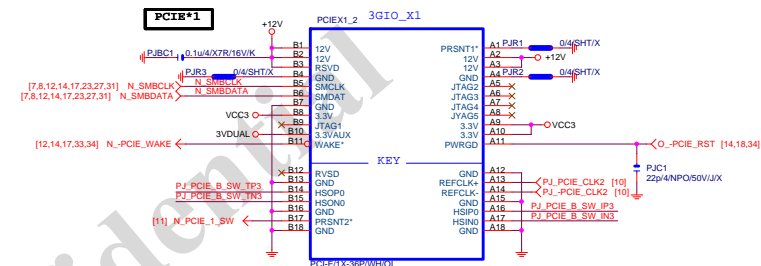
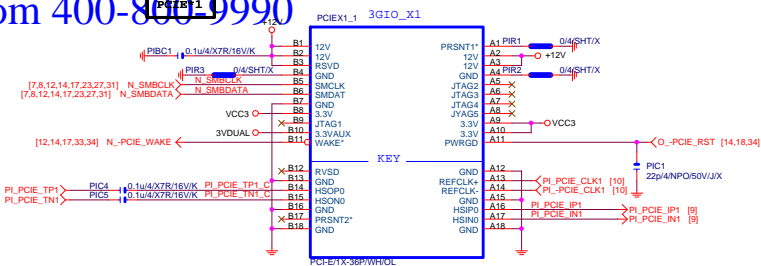
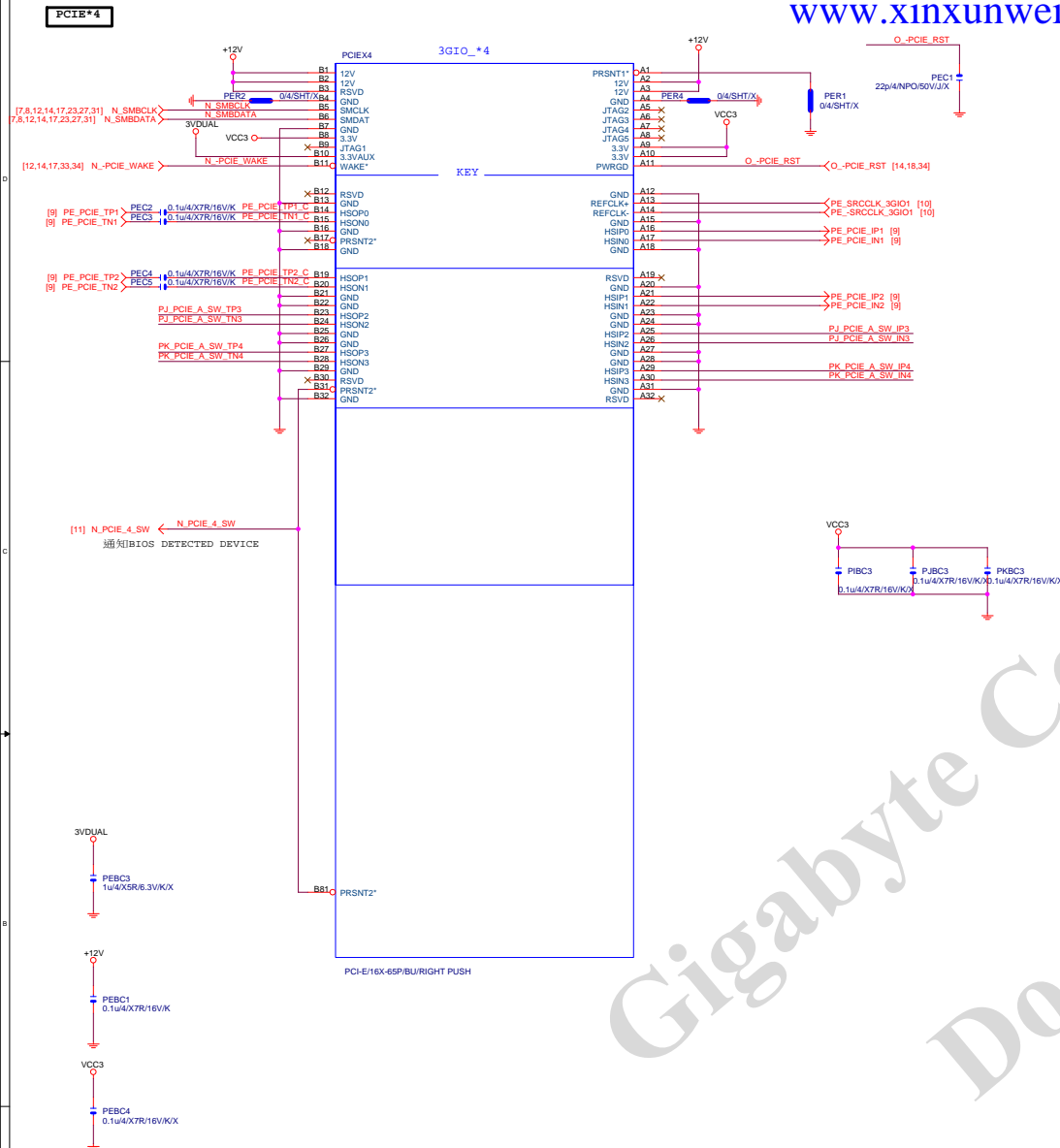






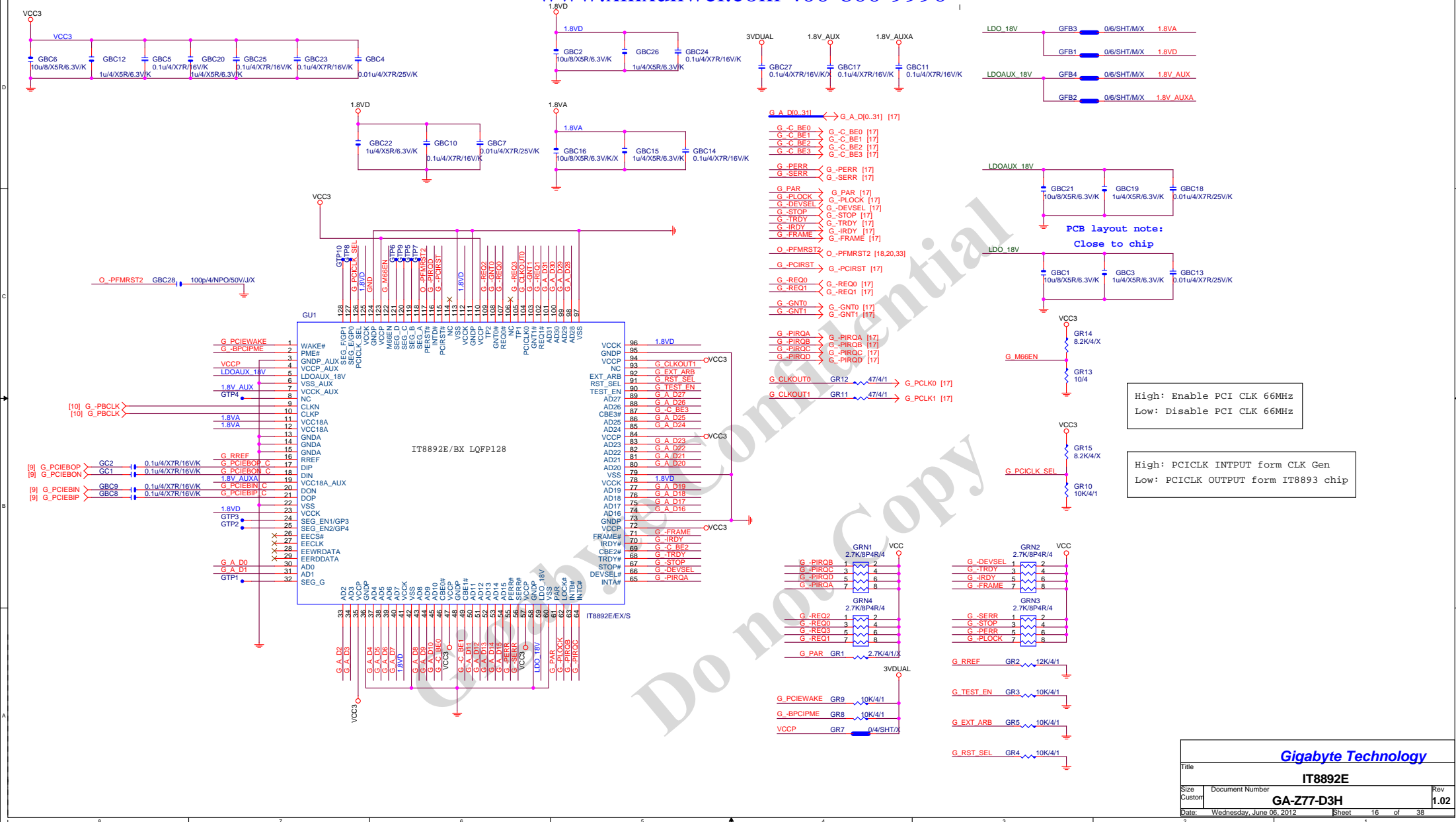
PCI-E REV:2.0--&gt; 5GHZ





	N_PCIE_4_SW (PCH GPIO38)	PCIE4_X1 (SIO GPIO26)
PCIE1,PCIE4 --> X1 ( Default )	H	H
PCIE4 No devices PCIE4 -> X1	H	H
PCIE4 Have devices PCIE4 -> X4 PCIE1_2/PCIE1_3 --> N/A	L	L

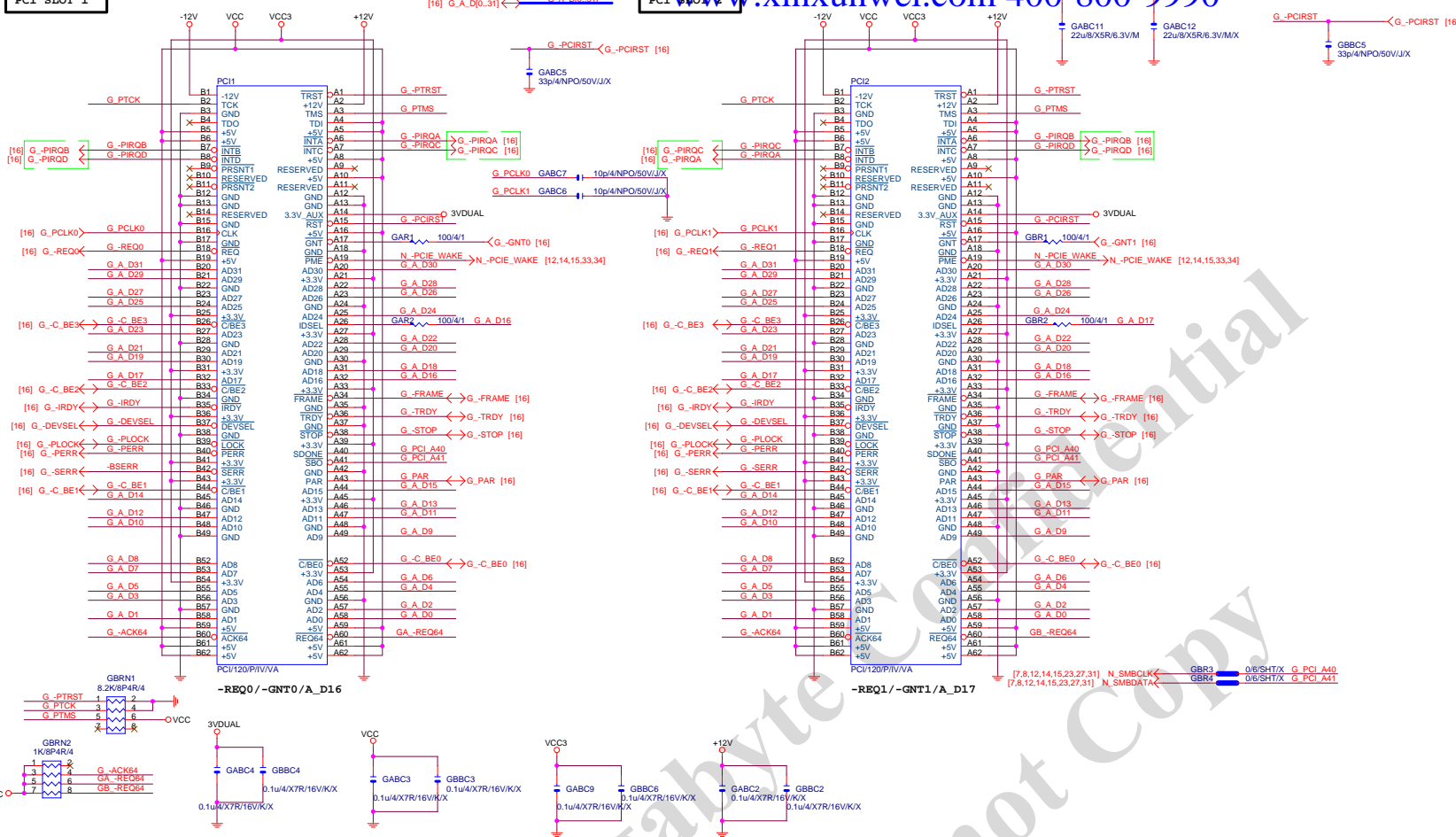
Function	SEL
xI--> x0a	L;PCIEX4 SLOT-->X1
xI--> x0b	H;PCIEX4 SLOT-->X4

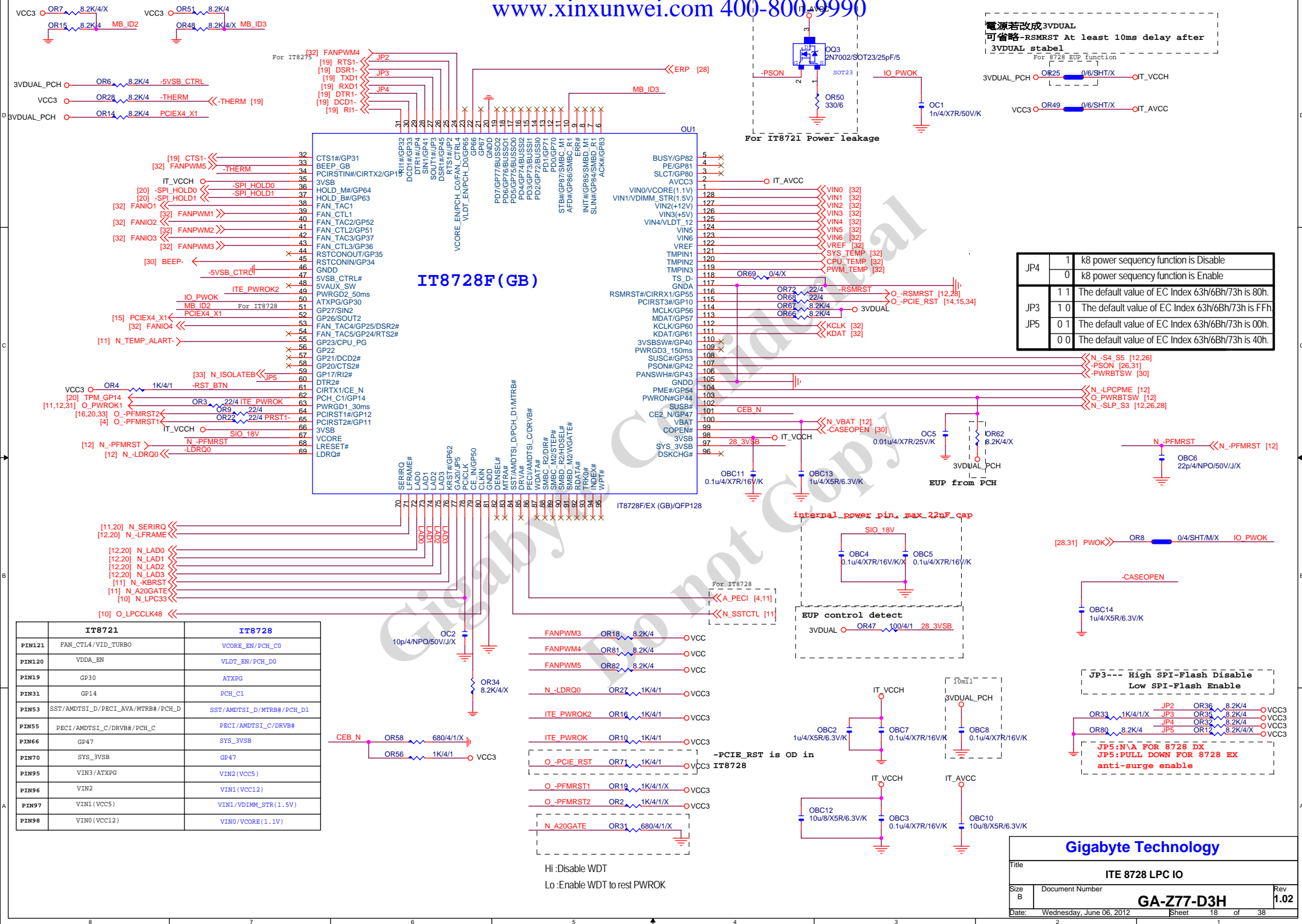


PCI SLOT 1

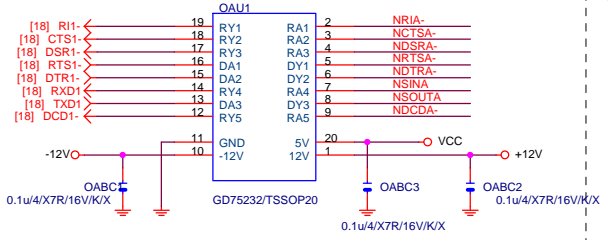
PCI SLOT 2

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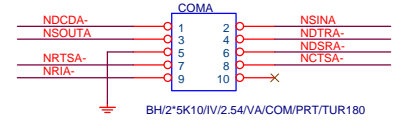
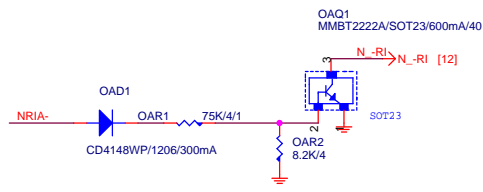




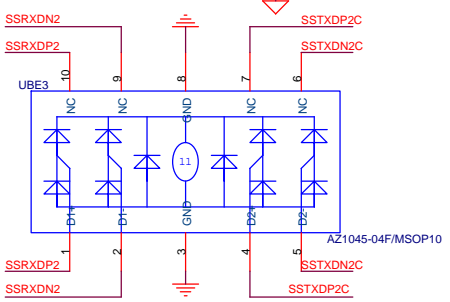
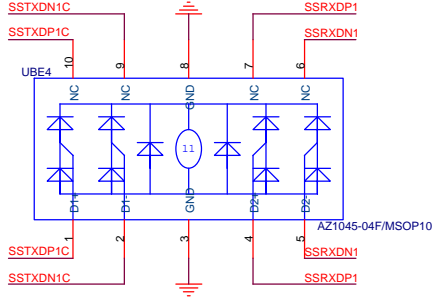
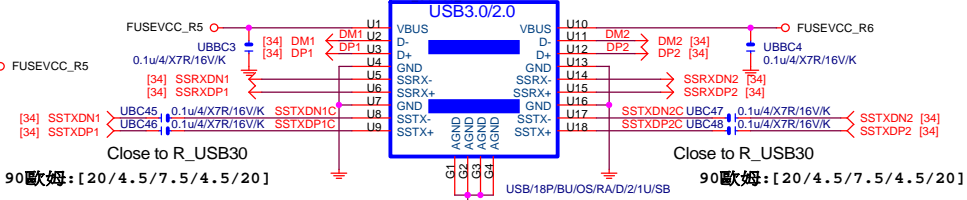
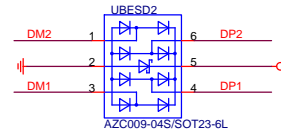
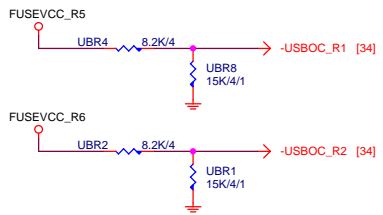
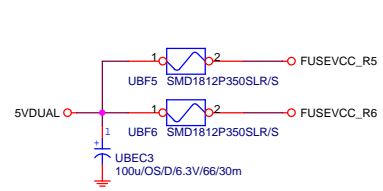
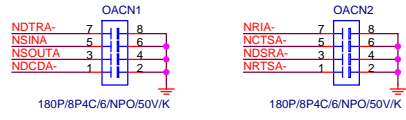
COMA



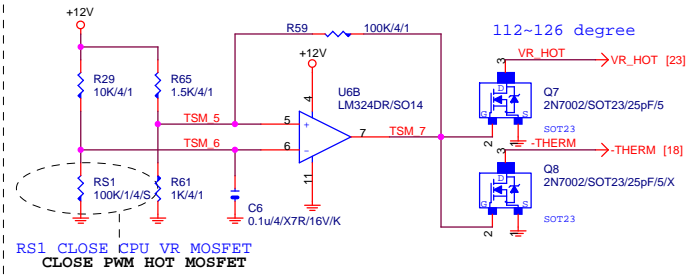
COM R1



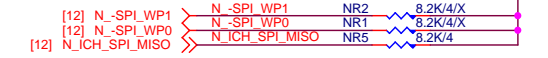
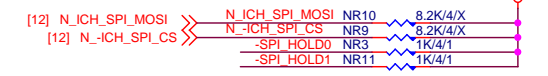
11NH3-000205-Y1R/Y2R



-PROHOT



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Title			
COM & PROHOT/Dynamic O.C.			
Size	Document Number	Rev	
Custom		GA-Z77-D3H	
Date:	Wednesday, June 06, 2012	Sheet	19 of 38

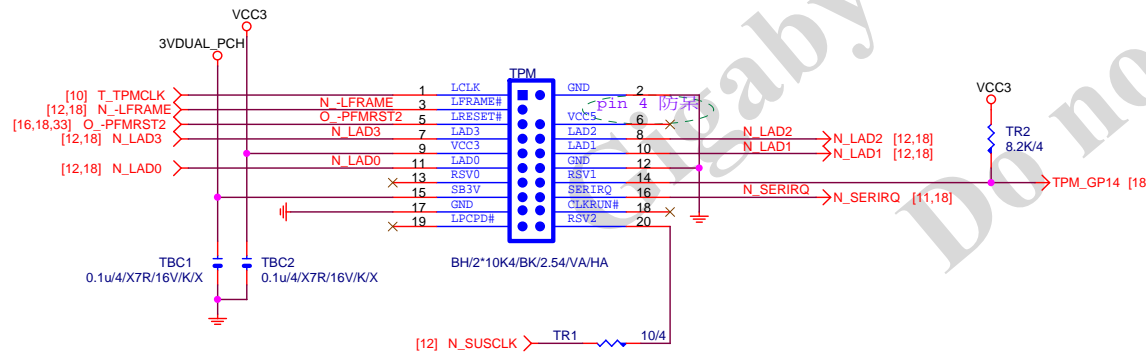
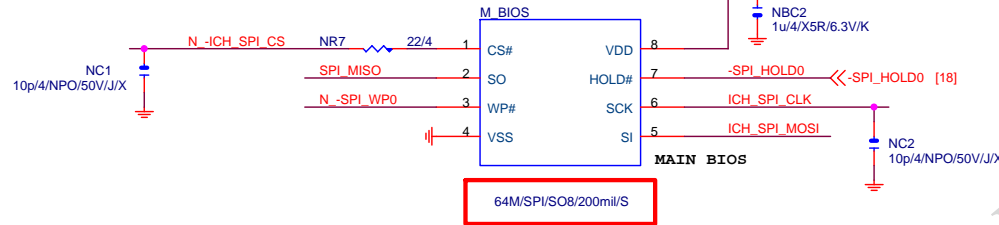


Default int pull up



BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

1 means floating  
 0 means PD 1K



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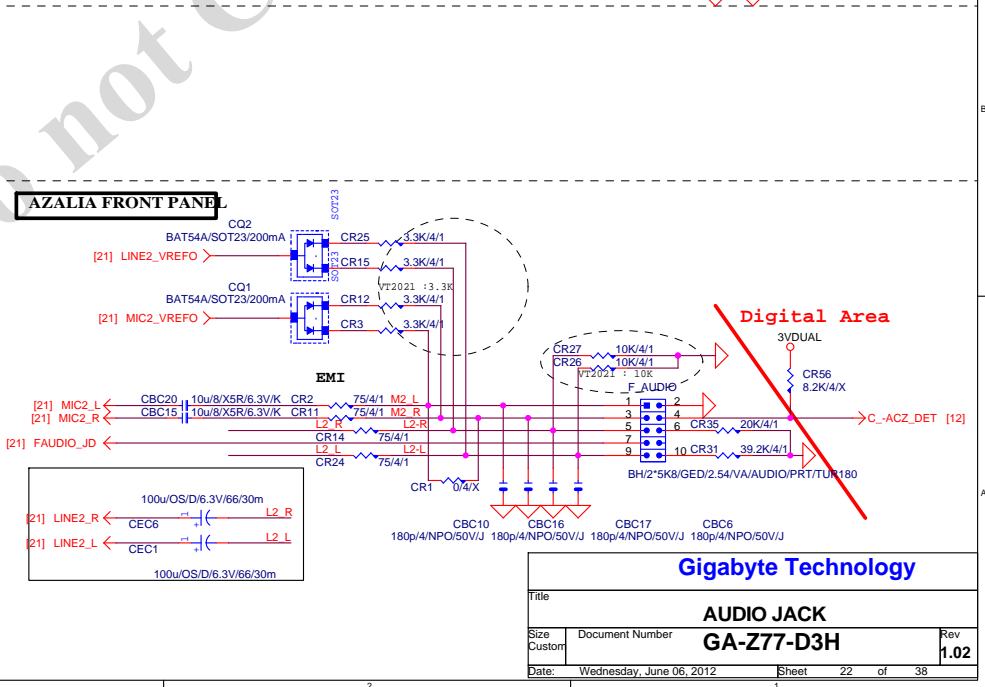
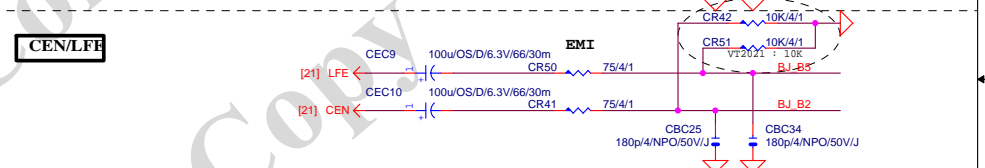
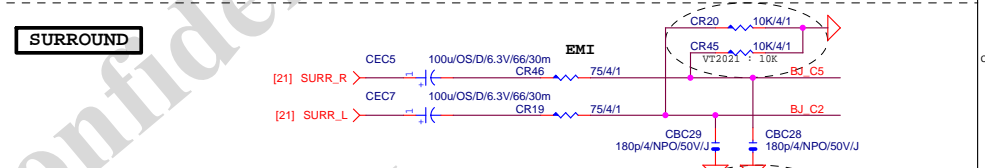
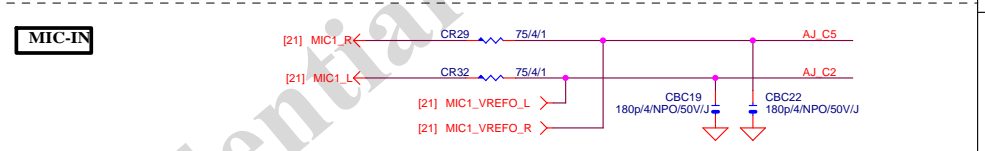
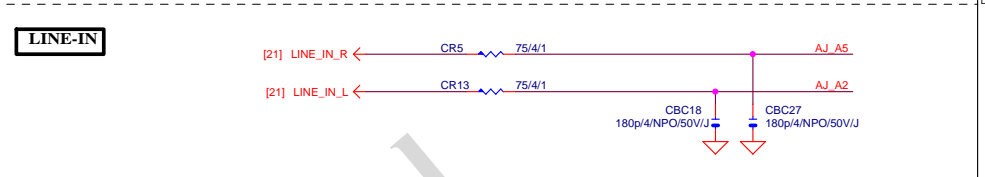
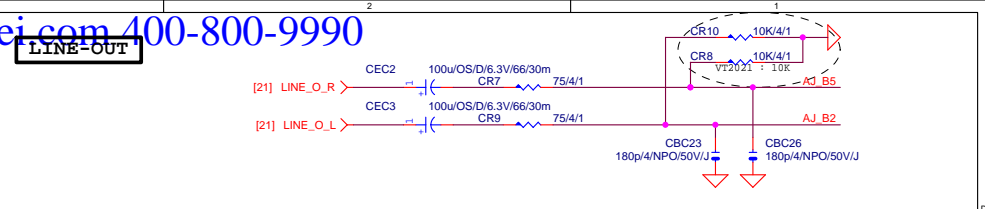
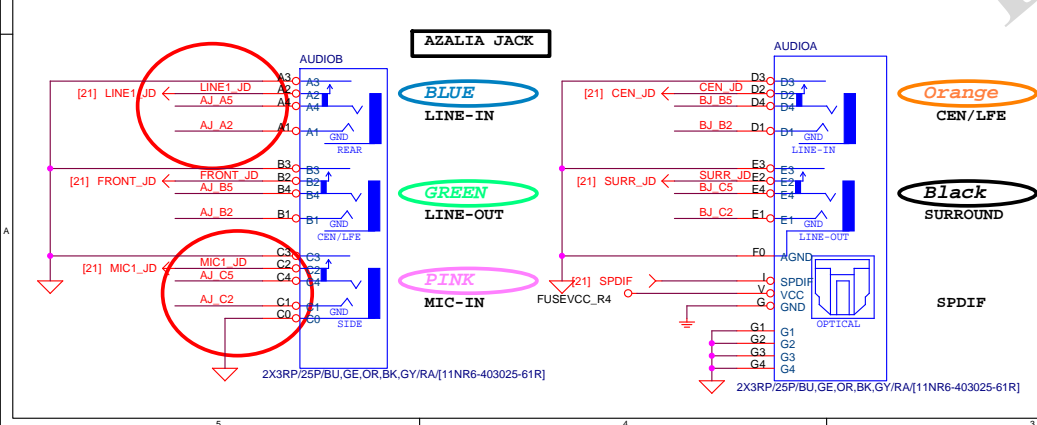
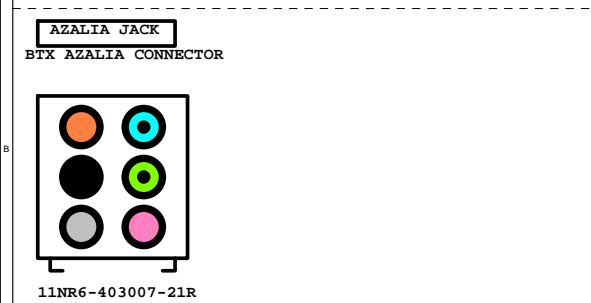
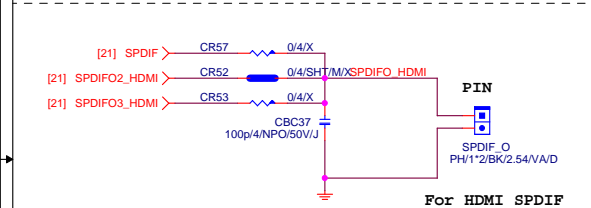
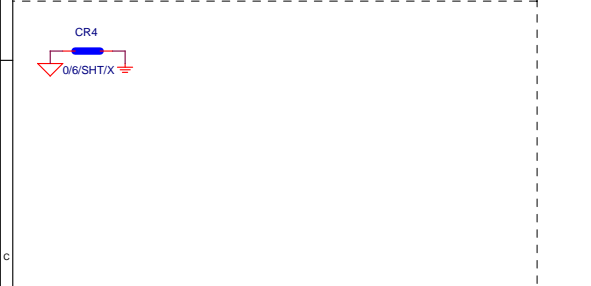
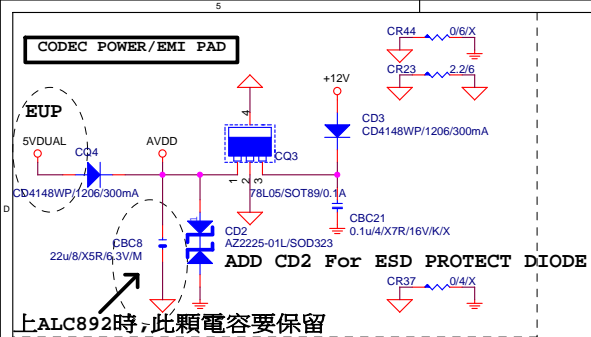
Title			BIOS
Size	Document Number	GA-Z77-D3H	
Custom		Rev	1.02
Date:	Wednesday, June 06, 2012	Sheet	20 of 38



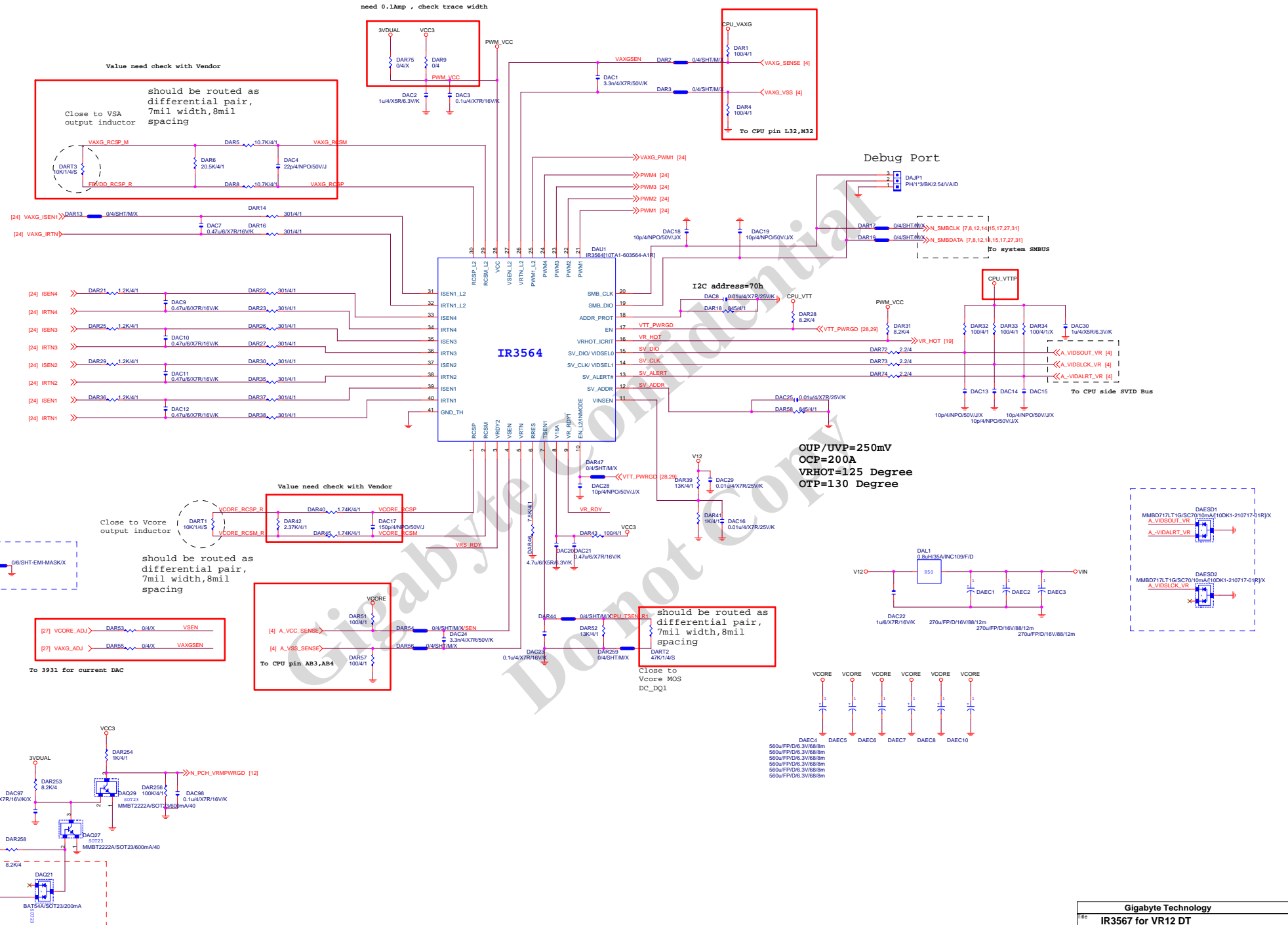
```
CR36: 20K/4/1% @Realtek cdec & VT1708S-CE
CR36: 5.1K/4/1 @VIA codec VT1708S-CD/VT2021
CBC38 100P @VIA codec VT1708S
```

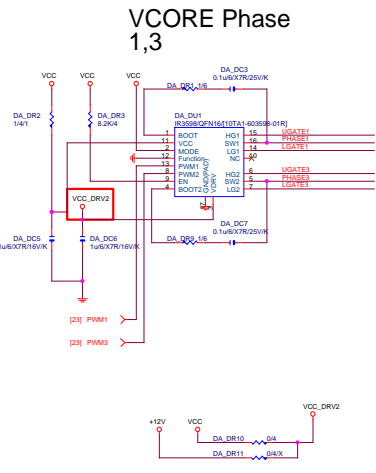


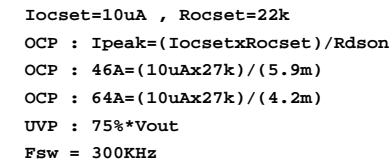
Title		HD AUDIO VT2021	
Size	Document Number	GA-Z77-D3H	Rev
Custom			1.0
Date:	Wednesday, June 06, 2012	Sheet	21 of 38



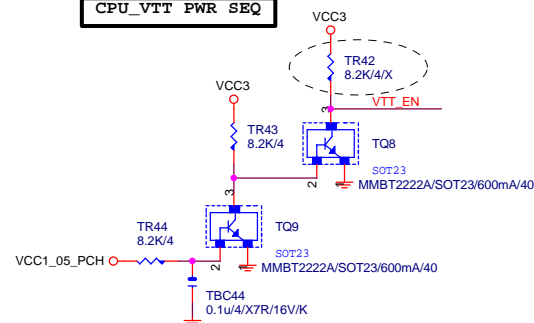
need 0.1Amp , check trace width



VCORE Phase  
1,3



CPU\_VTT PWR SEQ



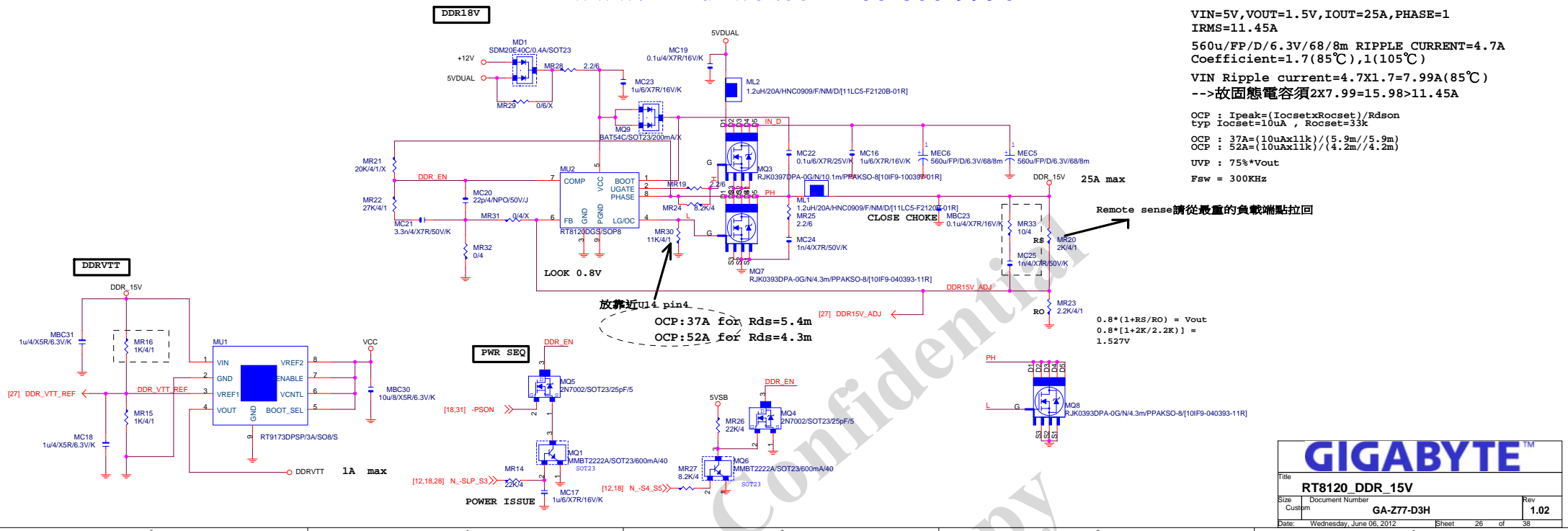
	VTT_SEL
HI	1.05V
LO	1.0V

According intel  
CDI/IBP#476733, 固定1.05V

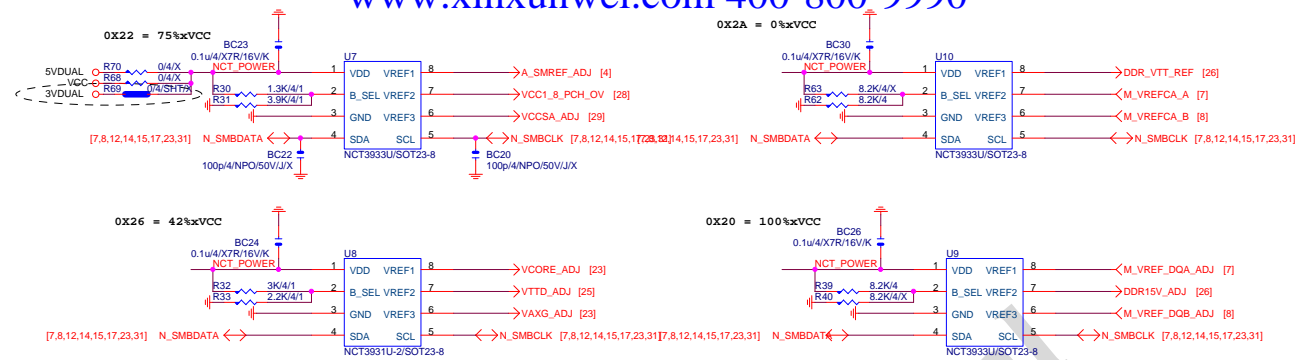
$$0.8 \cdot (1 + R_S/R_O) = V_{out}$$

$$0.8 \cdot [1 + 1.1K/3K] =$$

$$V_{out} = 1.09V$$



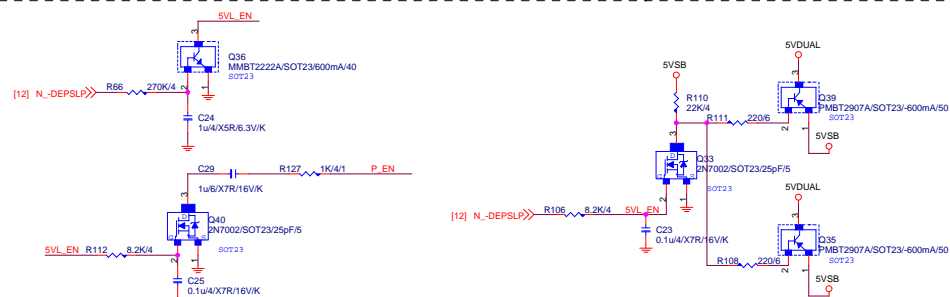
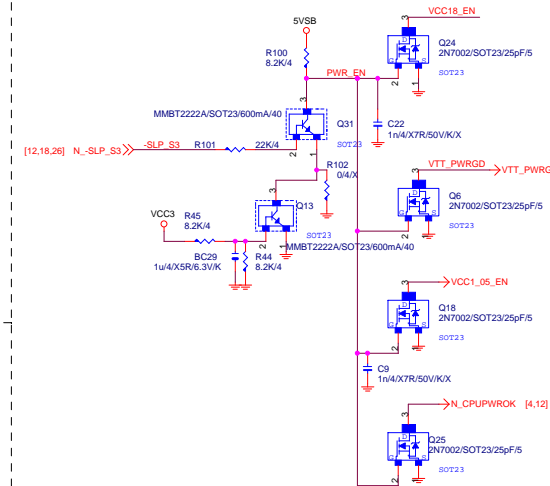
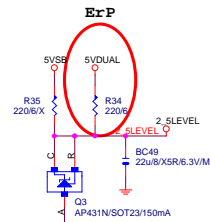
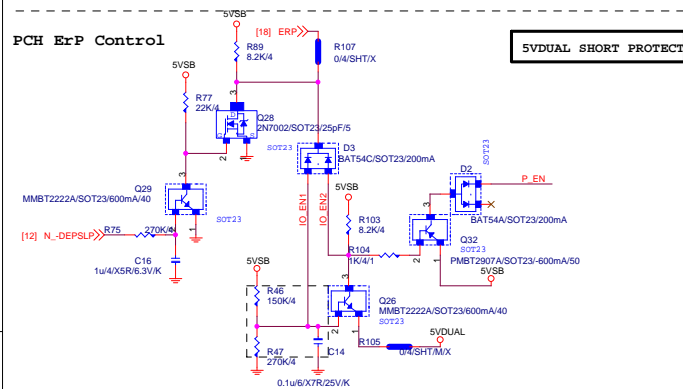
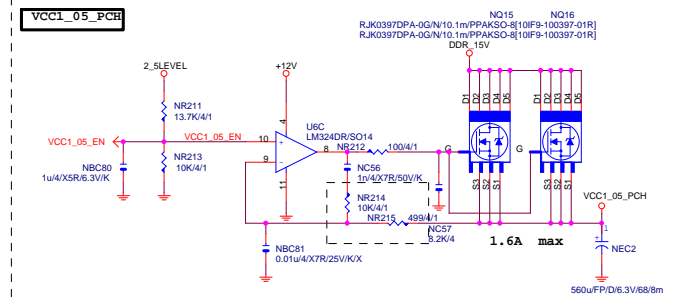
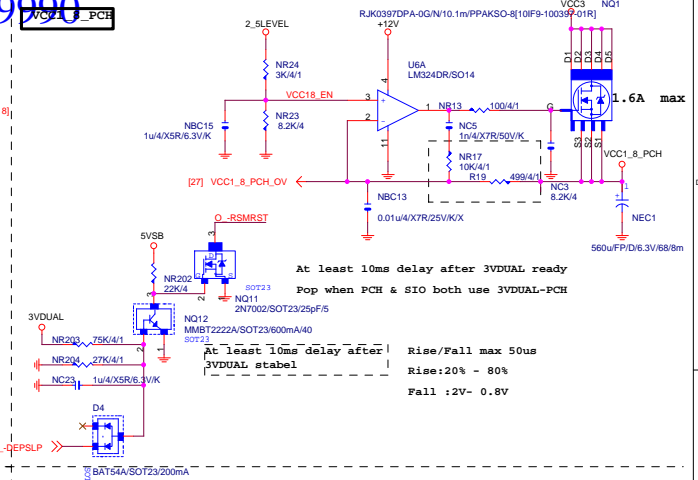
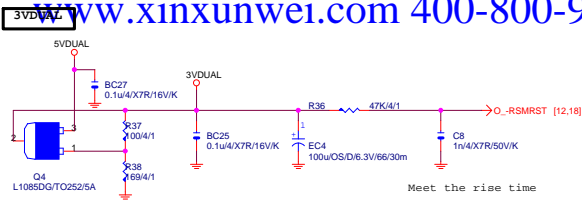
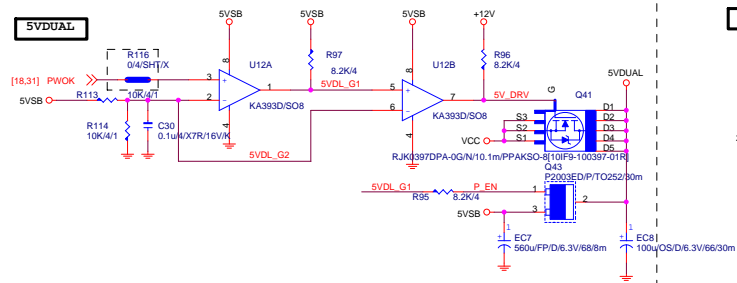




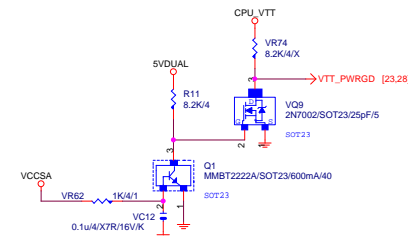
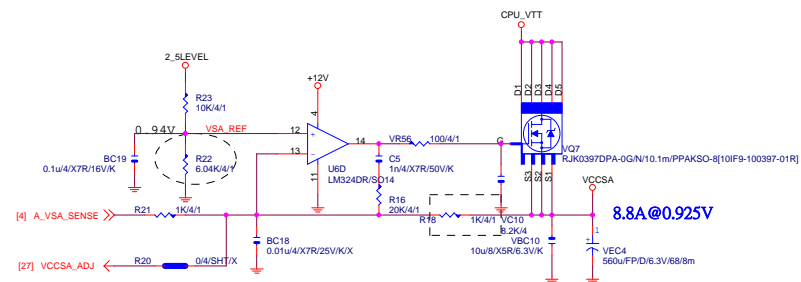
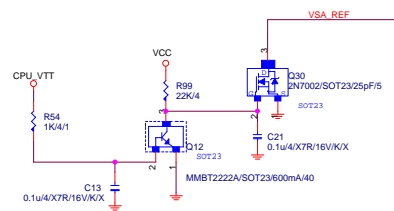
NCT3933	0X2A	0X20	0X22	0X26
VREF1	DDRVTT	VREF_DDRA_DQ	SMREF	VCORE
VREF2	VREF_DDRA_CA	DDR15V	VCC1_8_PCH	CPU_VTT
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	VCCSA	VAXG

Gigabyte Technology

Title			CPU CORE VR-2
Size	Document Number	GA-Z77-D3H	
Custom		Rev	1.02
Date:	Wednesday, June 06, 2012	Sheet	27 of 38



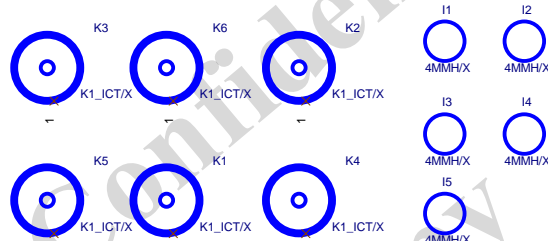
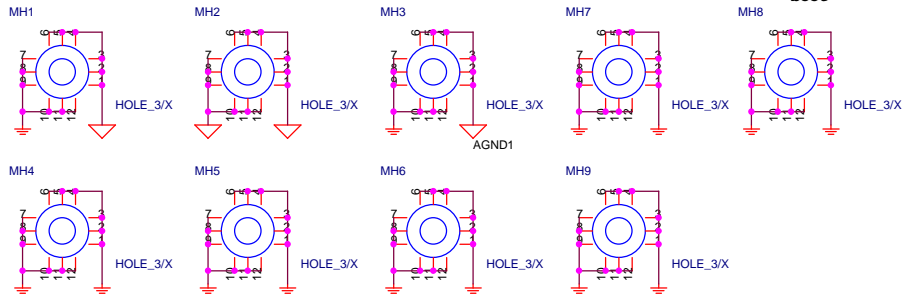
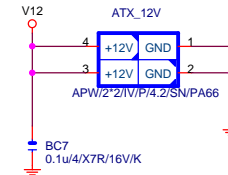
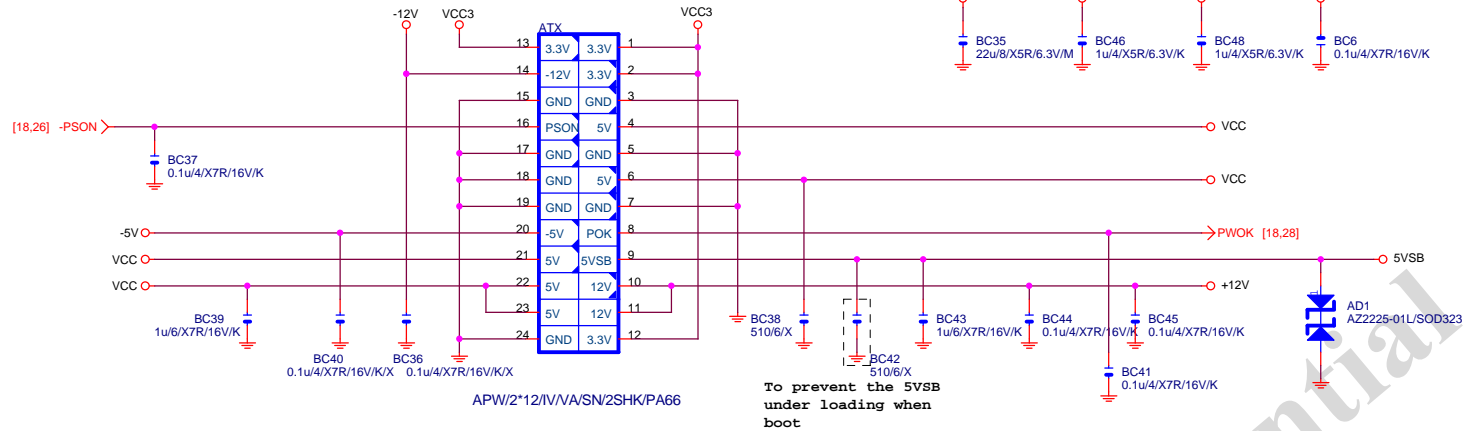
VCC\_SA



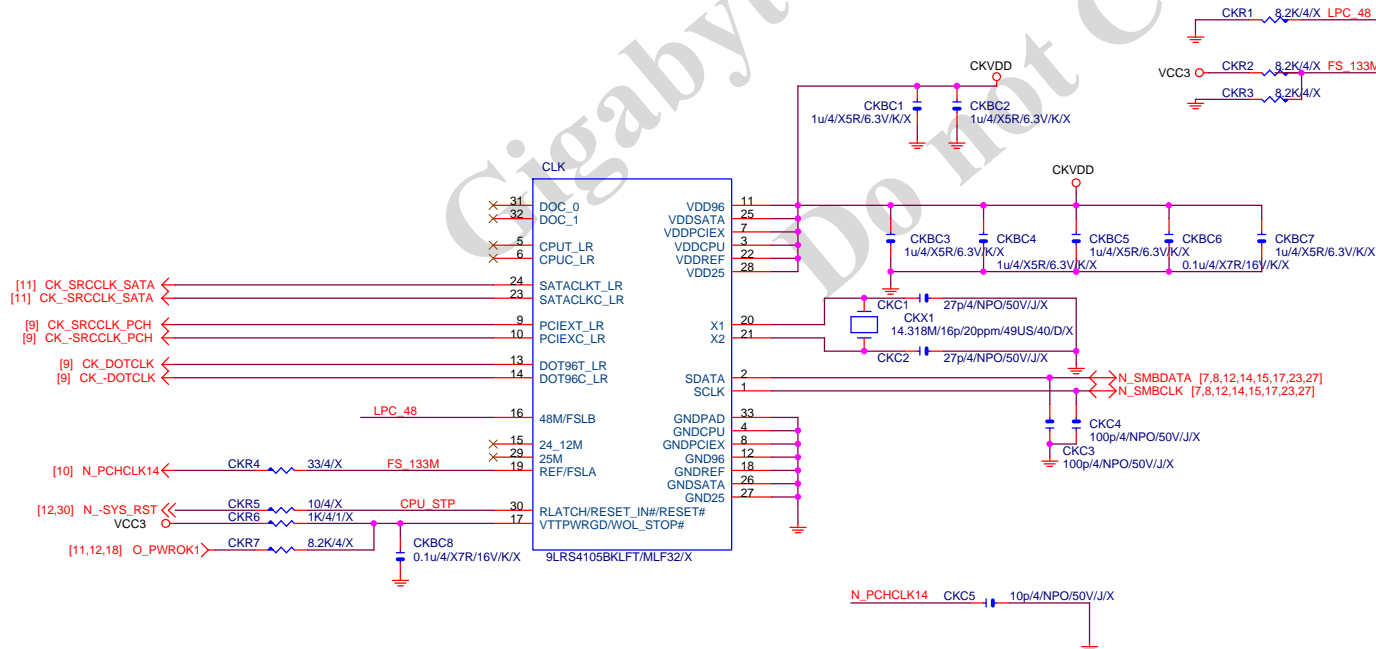


# ATX POWER CONNECTOR

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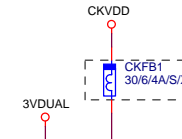


## CLK GEN



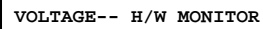
## CPU Frequency Selection

FS	CPU
0	100M <Default>
1	133M



## Gigabyte Technology

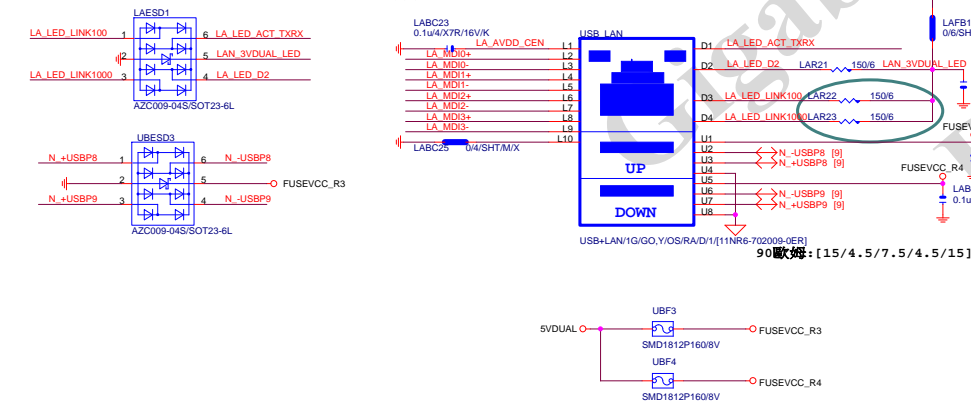
Title		ATX POWER CONNECTOR	
Size	Document Number	GA-Z77-D3H	
Custom		Rev 1.02	
Date:	Wednesday, June 06, 2012	Sheet	31 of 38



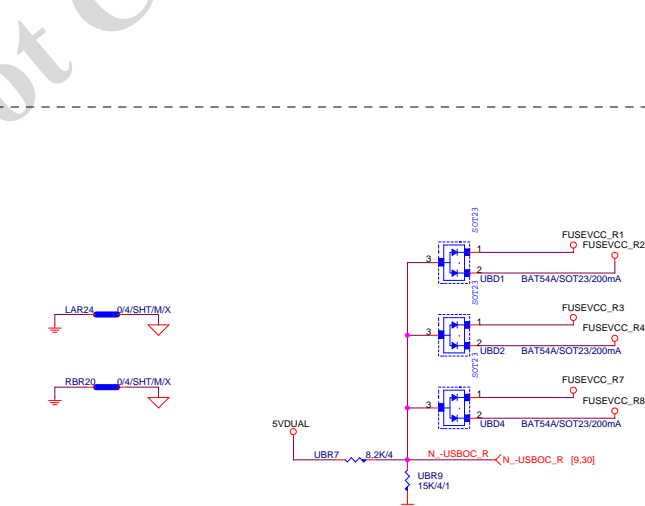
Title				HWM,KB/MS, FAN CTRL			
Size	Document Number						Rev
Custom	GA-Z77-D3H						1.02
Date:	Wednesday, June 06, 2012			Sheet	32	of	38



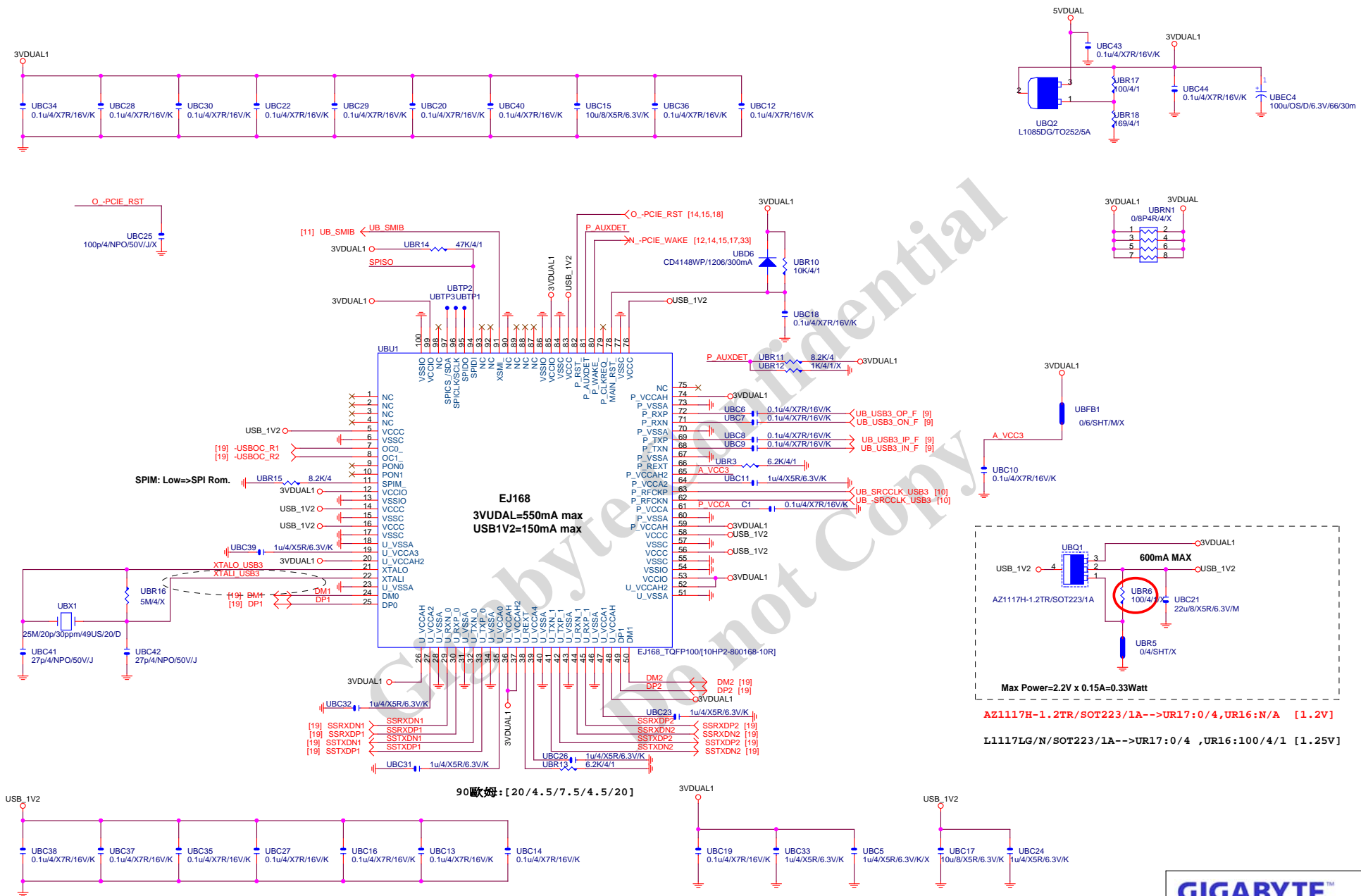
### USB30\_LAN CONNECTOR

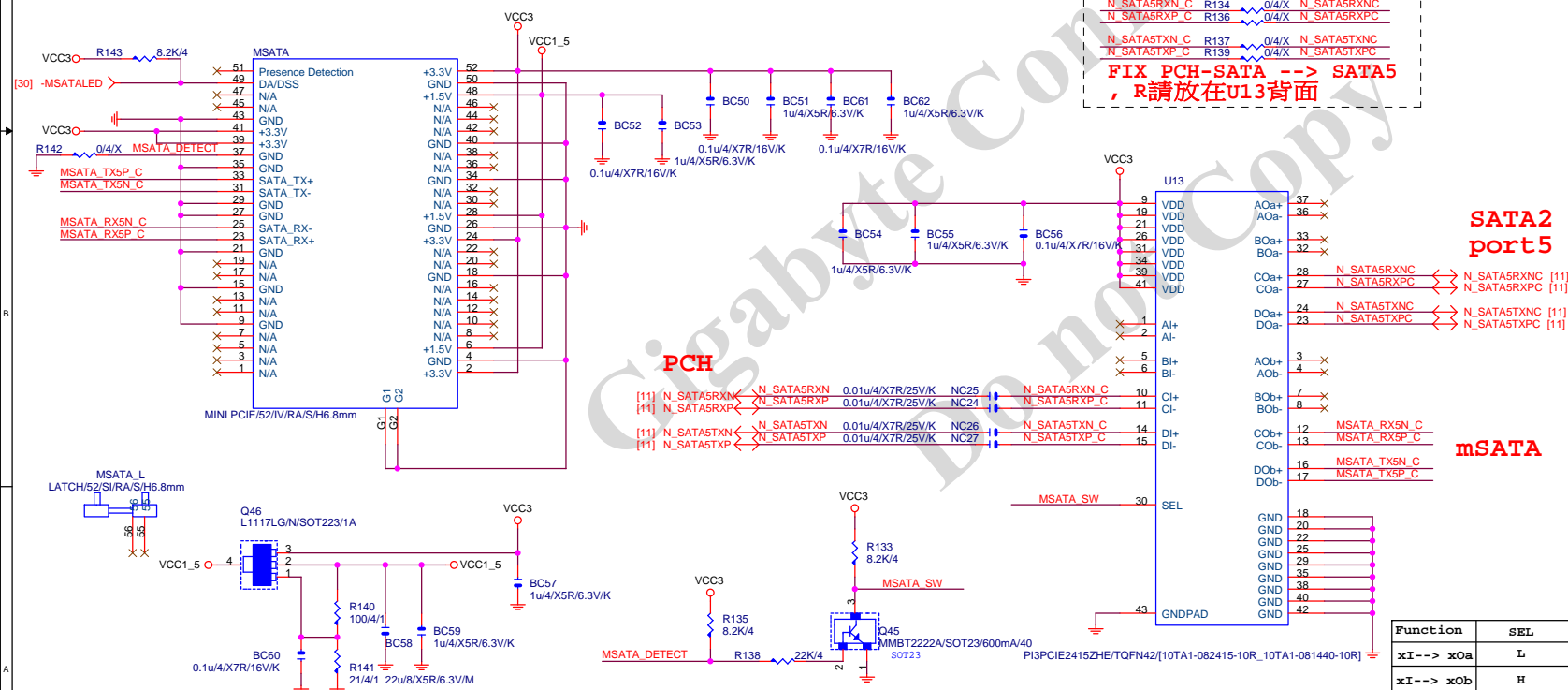


## MDI : AR8161--&gt;N/A



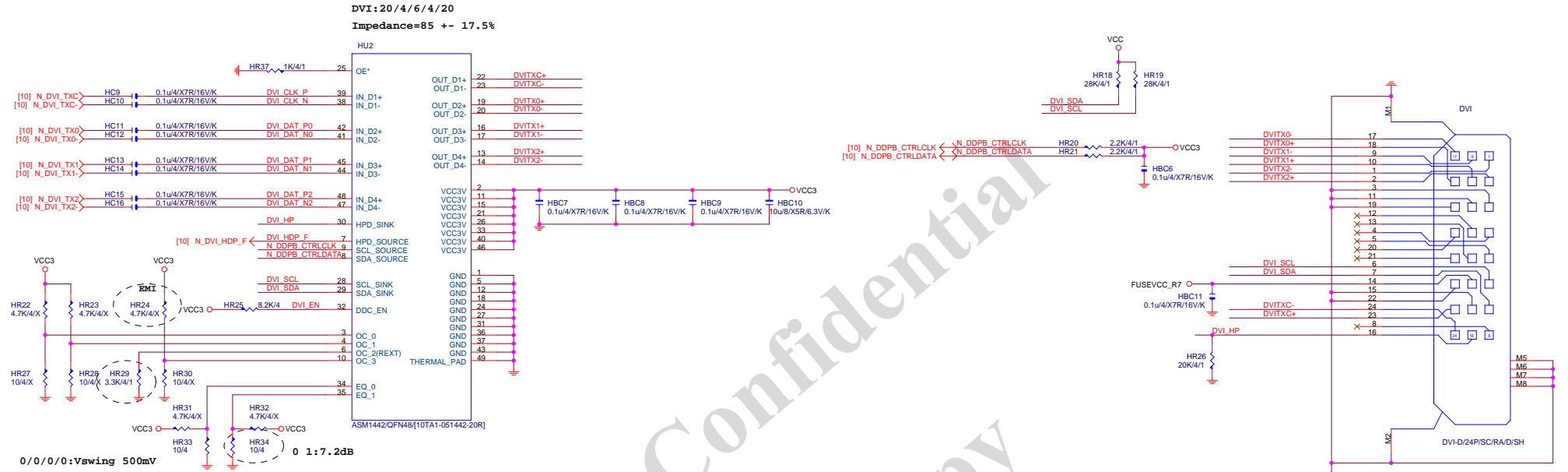
	AR8151	AR8161
AVDD33	N/A	3.3V
VDD33	3.3V	3.3V
AVDDH	2.7V	2.7V
AVDDL/DVDDL	1.1V	1.1V
VDDCT	1.7V	





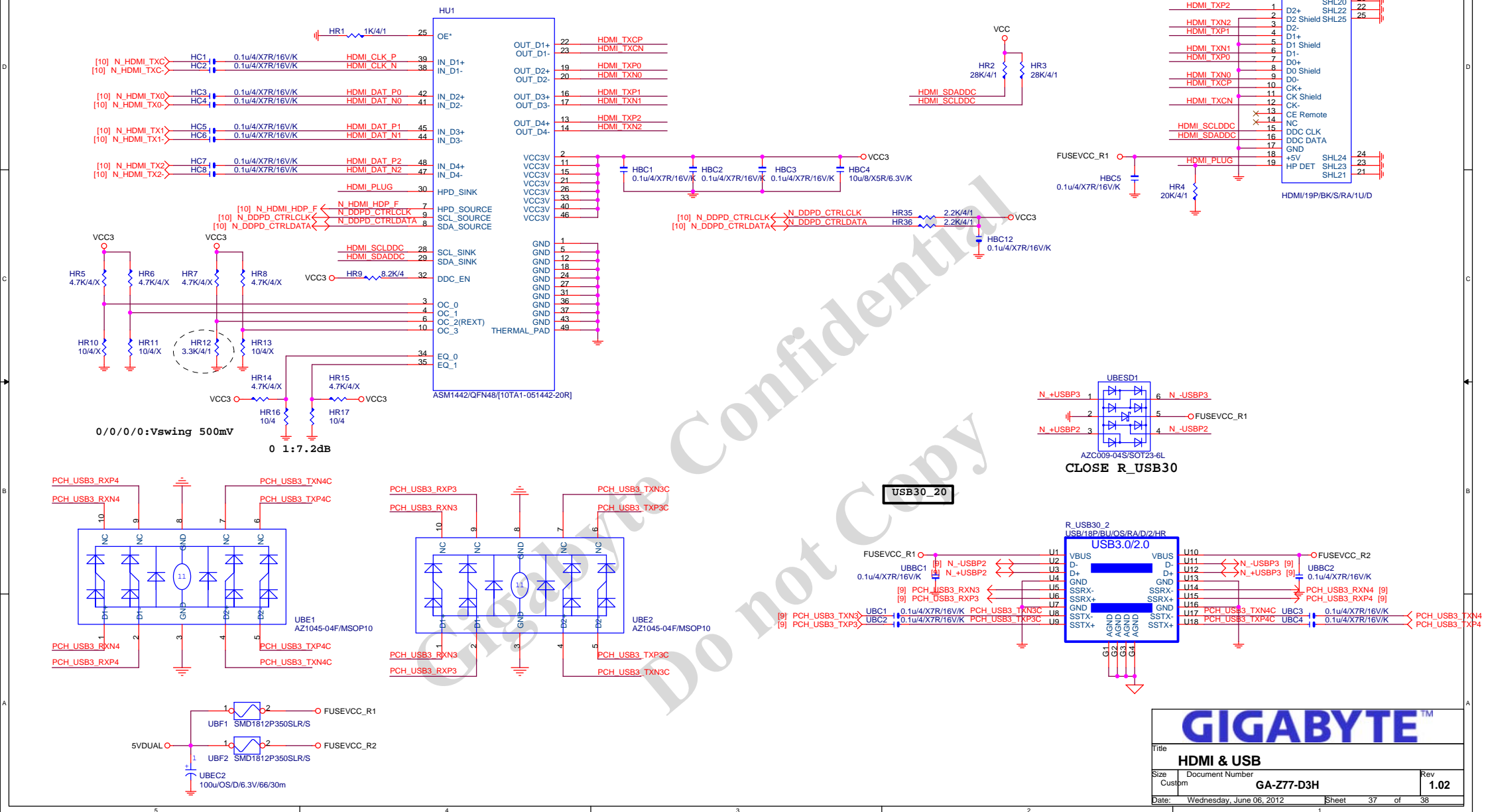
# GIGABYTE™

Title <b>VAXG PHASE</b>		
Size Custom	Document Number <b>GA-Z77-D3H</b>	Rev <b>1.02</b>
Date: Wednesday, June 06, 2012	Sheet 35 of 38	



Gigabyte Technology

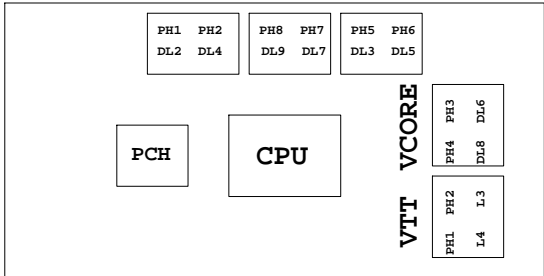
Title			TI TSB43AB23 1394
Size	Document Number	Rev	1.02
Custom	GA-Z77-D3H		
Date:	Wednesday, June 06, 2012	Sheet	36 of 38



Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRXL/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSS00	N/A	

PWM各相位的擺法如下：



BIOS超電壓對應表：

散熱模組料號:

8IBP:  
1.12SP2-01A001-Y1R/Y2R  
2.12SP2-01A001-Z1R/Z2R  
(HIBRID模組)包材階

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

<b><i>Gigabyte Technology</i></b>			
Title			
<b>TABLE LIST</b>			
Size	Document Number		Rev
C	<b>GA-Z77-D3H</b>		<b>1.02</b>
Date:	Wednesday, June 06, 2012	Sheet	38 of 38